DATA I/O

40-PIN GANG PROGRAMMING MODULE 950-0073-002

REV E JUNE 82 10-950-0073-002

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SECTION 1
INTRODUCTION

1.1 GENERAL INFORMATION

The Data I/O 40-Pin Gang Module provides the user with a simple method of programming up to eight 87XX-series microcomputers at a time. The 40-Pin Gang Module is adaptable to all Data I/O Universal Programmers (System 17 and 19, 29A and the Model 100A Production Programmer.) Other Data I/O programmers may later be added to this list.

NOTE

In order to program 40-pin microcomputer devices with the Gang Module, the Data I/O Port Multiplier must not be connected to the programmer. Also, do not use 12K extended programmer RAM with the Gang Module.

1.2 HOW IT WORKS

The 40-Pin Gang Module is designed to program different types of microcomputer devices. To program your specific device, simply select the appropriate Characterizer and insert it on the Gang Module. Each Characterizer tailors the Gang Module to the programming requirements of one device. The device number appears on the housing of the Characterizer. Table 1-1 provides a list of programming applications for the Gang Module.

Once the Gang Module has been installed on the programmer, the programmer will perform all normal functions as usual. Those functions that you will typically use with the 40-Pin Gang Module are: Load, Program, and Verify.

To load, insert your device into the master socket. Then, add up to eight blank devices for programming. Before programming, the Gang Module will perform a blank check and an illegal bit check on each device. While the devices are being simultaneously programmed, an LED indicator will light if any of the parts are unacceptable. After the batch of devices has been programmed, the programmer will verify the data in each device against the data in RAM to make sure all the devices were programmed successfully.

Table 1-1. Programming Applications for the 40-Pin Gang Module*

DEVICE NUMBER	CHARACTERIZER P/N
8741A	714-1860-001
8748	714-1860-002
8748H	714-1860-005
8749H	714-1860-006
8755A	714-1861-001

* Check your latest Data I/O *Comparison Chart of Programmable Devices* for later additions to this list.

1.3 SPECIFICATIONS

1.3.1 CONTROL ELECTRONICS

The Gang Module receives its power from the programmer. The module generates programming waveforms from raw supplies in the programmer, using regulators controlled by the programmer's microprocessor. The controlling software is located in the Gang Module.

1.3.2 PHYSICAL AND ENVIRONMENTAL SPECIFICATIONS

Weight. 3 lb. 3 oz. (1.45 kg.)
Dimensions. 24 cm x 17 cm x 10 cm (9.5" x 6.7" x 4.2")
Operating Temperature Range. 0 to 40C (32 to 104F)
Storage Temperature Range. −40 to 55C (−40 to 131F)

1.4 CALIBRATION

The need for calibration varies with the amount of use. Generally, we suggest calibration whenever programming yields fall below device manufacturers' recommended minimums.

The Gang Module can be calibrated only with a programmer that has an address and data display; Gang Modules used with a System 17 Programmer must either be calibrated on a Universal Programmer with keyboard display or sent to a Data I/O Service Center.

1.5 WARRANTY

Data I/O equipment is warranted against defects in materials and workmanship. The warranty period on the Gang Module is 90 days and begins when you receive it.

The warranty card inside the back cover of this manual explains the warranty.

1.6 SERVICE

Data I/O maintains service centers throughout the world. Each facility is staffed with factory trained technicians to provide prompt, quality service. In addition to repairs, all Data I/O products are calibrated and cleaned.

For more information about servicing your Data I/O products, contact your Data I/O representative. A list of sales and service offices is included at the back of this manual.

1.7 ORDERING

To place an order for equipment, contact your Data I/O sales representative.

Orders for shipment should contain the following information:

- Description of the equipment. (See the latest Data I/O Price List or contact your sales representative for equipment and part numbers.)
- Quantity of each item ordered.
- Shipping and billing address of firm, including zip code.
- Name of person ordering the equipment.
- Purchase order number.
- Desired method of shipment.

SECTION 2
INSTALLATION

2.1 INTRODUCTION

The Gang Module was tested both electrically and mechanically before it was shipped, and was carefully packaged to prevent shipping damage. It should arrive free of defect, and in perfect operating condition. Carefully inspect the unit for any damage that may have occurred in transit; if you note any damage, file a claim with the carrier and notify Data I/O. Also be sure you have the equipment listed in Table 2-1.

Table 2-1. Supplied and Optional Equipment

PART	DATA I/O P/N
40-Pin Gang Programming Module	950-0073-002
40-Pin Gang Socket Assembly	750-1502-001
Characterizer(s)	714-XXXX-XXX*
Calibration Extender†	910-1521

* The number of Characterizers and their part numbers vary from order to order.

† Required for Calibration only.

2.2 INSTALLING THE GANG MODULE

The Gang Module mounts easily onto the Data I/O Programmer.

Install the Gang Module by inserting the flange on the top edge of the programmer opening and pressing firmly on the bottom of the module to ensure a good connection between the units.

2.3 INSTALLING THE CHARACTERIZER

Select the proper Characterizer for the type of device to be programmed. (The appropriate characterizer manual provides complete information.)

CAUTION

Devices can be damaged if the wrong Characterizer is installed during a program or verify operation.

Install the Characterizer by pressing it into the socket so that the device number (*e.g.*, 8741 or 8748) is forwards. The Characterizer can be inserted in only one direction.

Characterizers may be installed or removed while the programmer's power switch is on and no operation is in effect.

2.4 REPACKAGING FOR SHIPMENT

If you need to ship your Gang Module to Data I/O for service or repair, attach a tag to it describing the work required and identifying the owner. In correspondence, identify the unit by part number and name.

If you use the original shipping container, place the instrument in the container with the appropriate packing material and seal the container with strong tape. If you use another container, be sure that it is a heavy carton, wrapped with sturdy plastic or paper. Use appropriate packing material and seal the carton well with strong tape. Mark the container "DELICATE INSTRUMENT" or "FRAGILE."

SECTION 3
OPERATION

3.1 INTRODUCTION

This section describes the three device-related operations possible with the 40-Pin Gang Module: Load, Program and Verify.

3.2 PREOPERATION PROCEDURES

CAUTION

Follow the procedures in paragraphs 3.2.1 - 3.2.3 to avoid damage to the programmer, Gang Module, or devices to be programmed.

3.2.1 COMPATIBILITY OF COMPONENTS

Make sure you have the right Characterizer for the type of device to be programmed. Refer to the appropriate Characterizer manual for further information.

3.2.2 TURN-ON

Install the Gang Module according to the procedure in Section 2.

Turn the programmer on with the switch at the rear.

CAUTION

Voltage transients can damage devices. Be sure that no devices are installed in the sockets when switching power on and off and when installing or removing the Gang Module with power on.

Never install or remove the Gang Module or Characterizer while an operation is occurring. The Gang Module and Characterizer may be installed with the programmer's power switch on. This feature allows RAM data to remain intact during changes of equipment.

3.2.3 DEVICE INSERTION

A good electrical connection between the device and socket is essential. Device pins must be clean and undamaged. Insert the device in the socket with the socket lever upright, and pin 1 of the device in pin 1 of the socket. Lock the device in the socket by pushing the lever down.

CAUTION

Never insert or extract a device during a Program, Load, or Verify operation.

3.3 OPERATIONS

The three device-related operations possible with the Gang Module are Load, Program and Verify. These are described in the following paragraphs.

3.3.1 MODE SELECTION

First, set up any desired operating parameters on the programmer. Then, select the desired mode: Load, Program or Verify. Start the operation by pressing START.

Make sure that the programmer signals the end of the operation before removing any installed devices.

If an error occurs during an operation, the programmer will either: 1) halt at the address where the error has occurred and signal an error, or, 2) complete the operation and signal the error. Any decisions required of the operator are prompted by a flashing display. A list of error codes is provided in Table 3-1.

3.3.2 LOADING DEVICE DATA IN RAM

In a Load operation, data in the device in the master socket is placed in RAM. To execute a Load operation, follow the preoperational procedures of paragraph 3.2 and then these steps.

1. Insert the Characterizer for the master device.
2. Insert the master device in the master socket, ensuring that it is correctly oriented.

NOTE

Remove any devices from sockets 2 through 8, as a faulty device in one of those sockets could affect the integrity of the data transfer.

3. Press START.

When all of the data has been transferred, the programmer will signal the end of the operation. All socket LEDs will be off.

3.3.3 PROGRAMMING DEVICES

In a Program operation, data in RAM is programmed into all installed devices. To execute a Program operation, complete the preoperational procedures in paragraph 3.2 and then proceed as follows.

1. Install the appropriate Characterizer.
2. Carefully insert the blank devices to be programmed in the Gang Socket Adapter. From 1 to 8 devices may be installed.
3. Press START.

Table 3-1. 40-Pin Gang Module Error Codes

ERROR CODES		
CODE	NAME	DESCRIPTION
21	Illegal-Bit Error	The device cannot be programmed due to already programmed locations of incorrect polarity.
31	Excessive Current Drain	The operation aborted due to excessive current drain by a device.
32	Backwards Device	A device may be in its socket backwards.
34	Faulty Characterizer	The operation aborted due to a faulty or inappropriate Characterizer.
35	Faulty Chip Select	The operation aborted due to data being present while a device is disabled.
38	Calibration	The operation aborted due to an invalid operation while in calibration mode.

During the operation the status indicators will show which stage of the automatic programming sequence is in effect. The stages are:

Test. The programmer first performs an illegal-bit test on all devices. If any device contains an illegal bit, the programmer will halt and the LED for the device will light. This device must be removed before the Test stage can be completed.

Remove or replace the device and initiate the Program operation again.

Next, the programmer performs a blank-check. If a device contains any programmed bits, the corresponding socket LED will light and programming will halt. LEDs for all sockets with blank devices will remain off.

NOTE

If a VOH device (e.g., 8741, 8748, 8749) has already been programmed and completely filled with Hex FF, it will be permitted to pass the illegal-bit test. This occurs because the Gang Module interprets it to be an empty socket. The devices will fail the subsequent blank-check test. If the operator attempts to program the device at this point, the device would also fail the verify operation at the end of the program cycle.

To continue the operation, press START.

Program. The devices are being programmed with data from RAM. The data display flickers to indicate that the operation is in progress. This stage can take several minutes.

Verify. Every address of each device is compared with the corresponding RAM data. If any mismatch occurs, the VERIFY light will flash.

Complete. If there are no verify errors, the programming cycle is complete.

3.3.4 DEVICE VERIFICATION

In a Verify operation, data at every device address is compared with the corresponding RAM data. To execute a Verify operation, complete the preoperational procedures in paragraph 3.2 and then proceed as follows.

1. Install the appropriate Characterizer.
2. Ensure that the devices are correctly inserted in the sockets.
3. Press START.

The programmer compares the device data for every device against RAM data, starting at socket eight and ending with the master socket. If a device verifies with RAM data, the corresponding LED will remain off. If the device in the master socket does not verify with RAM data, the LED will illuminate and the Verify operation will halt at the first nonverifying RAM address.

If a device other than the device in the master socket does not verify with RAM data, the corresponding LED will illuminate. The Verify operation will continue to completion.

SECTION 4
CALIBRATION

4.1 INTRODUCTION

Generally, the Gang Module should be calibrated whenever programming yields fall below device manufacturers' specifications. A "performance check" of calibration can be made with a digital voltmeter and the Measurement Chart.

If, after a performance check, voltage adjustments are required, complete the entire calibration procedure in this section or contact your local Data I/O Service Center.

A complete calibration consists of three parts:

- Measurement of the programmer's power supplies
- DC calibration
- Waveform observation

NOTE

The System 17 Programmer cannot be used to calibrate or make a performance check on the Gang Module.

The Gang Module is calibrated under the power of the programmer power supply. In addition, the following equipment is needed:

- Data I/O Calibration Extender, part number 910-1521
- Digital voltmeter (Fluke 8000A or equivalent)
- Dual-trace oscilloscope (Tektronix 465 or equivalent)

After successful calibration, the Gang Module should operate to specifications.

NOTE

Characterizers should not be installed during a performance check or during DC calibration.

4.2 PERFORMANCE CHECK OF DC CALIBRATION

To check DC voltages of the Gang Module, enter the Calibration Mode and use the Measurement Chart. The digital voltmeter is used to make the readings.

To make a performance check, leave the Gang Module installed as for normal operation. Paragraphs 4.2.1—4.2.3 tell how to make a performance check.

4.2.1 ENTERING THE CALIBRATION MODE

To enter, increment, decrement or exit the calibration mode, refer to the instructions in the programmer manual.

4.2.2 THE MEASUREMENT CHART

The Measurement Chart contains the information necessary for complete DC calibration. If the performance check yields voltages within the specified ranges, all supplies and drivers will have been fully tested, and the Gang Module will be ready for use.

The Measurement Chart presents calibration information as follows:

- The STEP NO. column tells which step to use for each test. Step numbers are set at the programmer keyboard.
- The TEST NO. column identifies the individual tests.
- The TEST DESCRIPTION column identifies the function being tested.
- The TEST LOCATION column tells which pins on the Master Socket or the Characterizer Socket to probe for measuring voltages.
- The VOLTAGE columns specify allowable voltage ranges. If a reading falls outside the range and cannot be adjusted to within the range, the Gang Module should not be used for programming.
- The ADJUSTMENT LOCATION column tells which potentiometer to adjust if a voltage is out of range.
- The COMMENTS column gives special instructions for particular tests.

4.2.3 MAKING DC-VOLTAGE MEASUREMENTS

Voltage readings are made at the device or Characterizer socket. Figure 4-1 shows the pin numbers for these sockets.

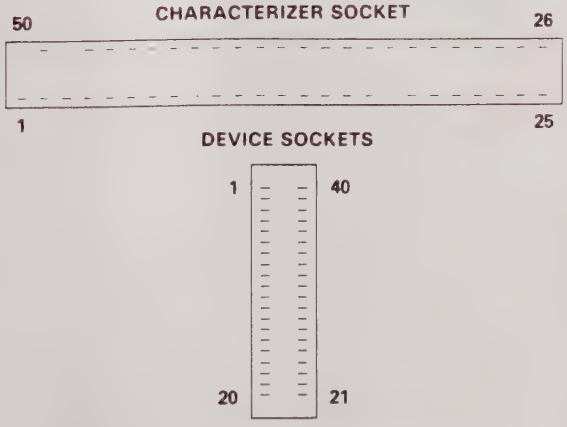

Figure 4-1. Pin Numbers of Device and Characterizer Sockets

Measurement Chart

PROGRAMMABLE DEVICE(S) 8741A, 8748, 8748H, 8749H, 8755A

PROGRAM ELECTRONICS 950-0073 SOCKET ADAPTER 750-1502-001

DATE	REV	REVISION RECORD	DR	CK
6/24/82	E	ECN #4607	EF	

STEP	TEST NO	TEST DESCRIPTION	TEST LOCATION Master Socket PIN(s)	TEST LOCATION Characterizer PIN(s)	VOLTAGES MIN	VOLTAGES NOM	VOLTAGES MAX	ADJUSTMENT LOCATION	COMMENTS
1	1	All voltages off	All	4,5,6	-0.40		0.65	N/A	
	2	Program pulse off	N/A	17	-0.20		0.20	N/A	
	3	All LEDs on	N/A	N/A				N/A	Confirm that all socket LEDs are on.
2	4	VDD = 25 V	N/A	4	24.5	25.0	25.5	R33	
	5	EA = 18 V	N/A	6	17.8	18.0	18.2	R38	
	6	Program pulse = 25 V	N/A	17	22.5	25.0	23.5	N/A	
	7	Vcc = 5 V	40	N/A	5.10	5.15	5.20	R36	Check all sockets.
	8	PGM = 0	N/A	5	-0.4		0.4	N/A	
	9	All LEDs off	N/A	N/A				N/A	Confirm that all socket LEDs off.
3	10	VDD = 21V	N/A	4	20.8	21.0	21.2	R33	If adjustment is required, recheck
	11	EA = 23 V	N/A	6	22.5	23.0	23.5	R37	test 4.
	12	PGM = 5 V	N/A	5	4.0		5.2	N/A	
4	13	VDD = 5 V	N/A	4	4.80	5.00	5.20	R7	
	14	EA = 5 V	N/A	6	4.00		5.20	N/A	
	15	Program pulse = 5 V	N/A	17	3.00		5.20	N/A	

NOTES:

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Measurement Chart

PROGRAMMABLE DEVICE(S) 8741A, 8748, 8748H, 8749H, 8755A

PROGRAM ELECTRONICS 950-0073 SOCKET ADAPTER 750-1502-001

DATE	REV	REVISION RECORD	DR	CK
		See sheet 1		

STEP	TEST NO	TEST DESCRIPTION	TEST LOCATION		VOLTAGES			ADJUSTMENT LOCATION	COMMENTS
			Master Socket PIN(s)	Characterizer PIN(s)	MIN	NOM	MAX		
5	16	Even address high	12,14,16,18,21	12	3.0		5.2	N/A	
	17	Odd address low	13,15,17,19,22	13	-0.4		0.4	N/A	
6	18	Even address low	12,14,16,18,21	12	-0.4		0.4	N/A	
	19	Odd address high	13,15,17,19,22	13	3.0		5.2	N/A	
7	20	Even data high	12,14,16,18	N/A	3.0		5.2	N/A	
	21	Odd data low	13,15,17,19	N/A	-0.4		0.4	N/A	
8	22	Even data low	12,14,16,18	N/A	-0.4		0.4	N/A	
	23	Odd data high	13,15,17,19	N/A	3.0		5.2	N/A	
9	24	PA 11 and 15 high	N/A	10,18	3.0		5.2	N/A	
	25	Others low	N/A	7,8,15,16,23,30	-0.4		0.4	N/A	
10	26	PA 10 and 14 high	N/A	16,30	3.0		5.2	N/A	
	27	Others low	N/A	7,8,10,15,18,23	-0.4		0.4	N/A	
11	28	PA 9 and 13 high	N/A	8,15	3.0		5.2	N/A	
	29	Others low	N/A	7,10,16,18,23,30	-0.4		0.4	N/A	
12	30	PA 8 and 12 high	N/A	7,23	3.0		5.2	N/A	
	31	Others low	N/A	8,10,15,16,18,30	-0.4		0.4	N/A	
13	32	All PA high	N/A	7,8,10,15,16,18,23,30	3.0		5.2	N/A	

NOTES:

DATA I/O

Connect the digital voltmeter as follows:

a. Connect the negative lead to ground on any Socket.

b. Connect the positive lead to the test points indicated on the Measurement Chart.

Follow the steps on the Measurement Chart in order.

CAUTION

If any voltages fall outside the limits on the Measurement Chart, do not use the Gang Module until it has been calibrated. Perform a complete calibration or contact your local Data I/O Service Center.

4.3 COMPLETE CALIBRATION

If, after a performance check, voltage adjustments are required, prepare for a complete calibration by installing the Data I/O Calibration Extender as described in this paragraph.

To perform a complete calibration, follow these steps in the order indicated:

a. Measure the programmer's power supplies as described in the appropriate programmer manual.

b. Perform the complete DC calibration (paragraph 4.5).

c. Observe waveforms paragraph 4.6.

First, follow the set-up procedure below and refer to Figure 4-2.

a. Remove the Gang Module from the programmer by lifting under the module gently to separate the connectors and then lifting it out.

b. Loosen the two captive screws which connect the Programming Electronics Assembly to the gang Socket Assembly, and separate the two units. The screws are located on the underside of the Gang Socket Assembly.

c. Install the Calibration Extender in the same way as the Gang Module, being sure to seat it properly in the programmer's mating connector.

d. Insert the 64-pin connector on the Programming Electronics Assembly into the mating connector on the Calibration Extender. The Gang Socket Assembly can then be most easily probed if it is laid flat on top of the programmer.

If a complete calibration fails to solve the problem, consult Section 6, *Troubleshooting*.

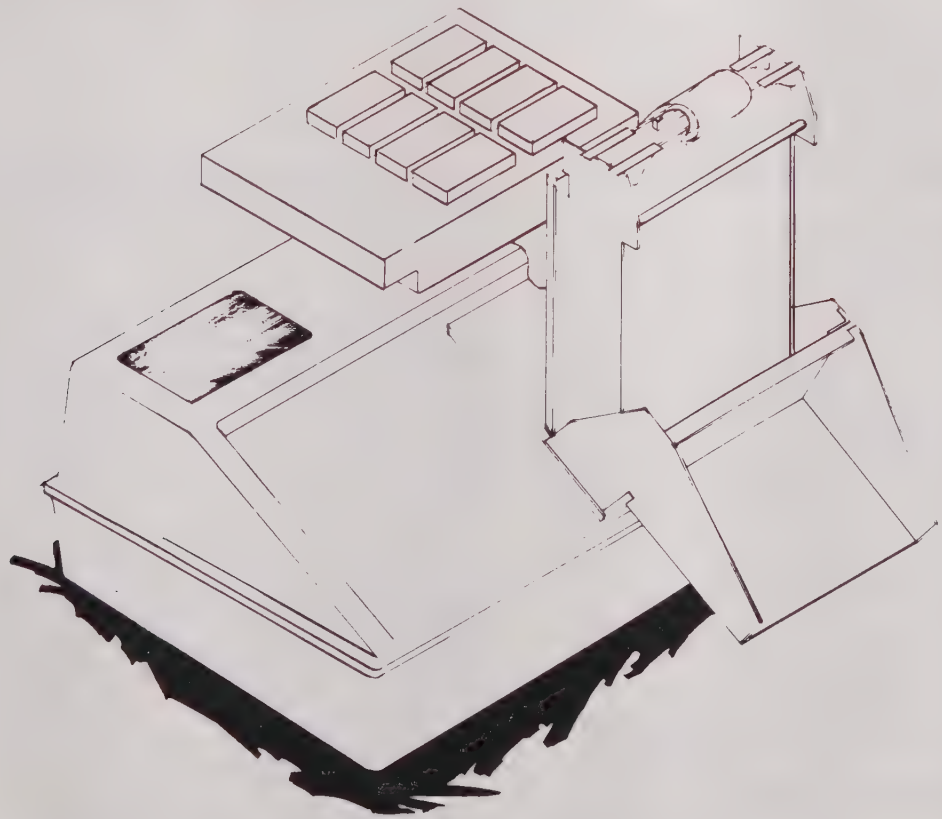


Figure 4-2. Gang Module Prepared for Calibration

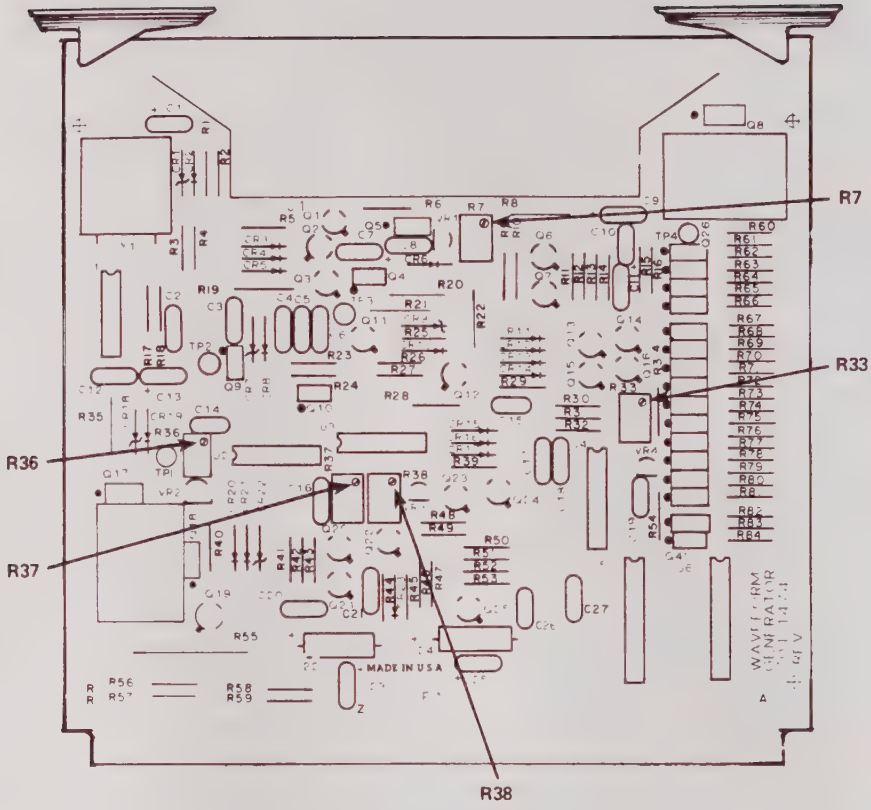


Figure 4-3. Calibration Adjustment Locations

4.4 POWER-SUPPLY MEASUREMENTS

To test or adjust the programmers power supplies, refer to the programmer Instruction Manual.

4.5 DC CALIBRATION

For DC calibration, again follow the steps on the Measurement Chart in order, making adjustments to bring voltages within the specified range.

Adjustments are made at the trim pots on the Waveform Generator Card, shown in Figure 4-3. These trim pots are accessible when the Gang Module is installed in the Calibration Extender.

4.6 WAVEFORM OBSERVATION

Programming waveforms can be observed with an oscilloscope and compared with the Timing Diagrams. In this way timing and magnitude relationships can be measured against known specifications to confirm that the Gang Module is performing to the PROM manufacturer's standards.

Since the Gang Module generates a large number of waveforms and all calibration adjustments are accomplished in DC calibration, we recommend observing waveforms only for PROMs that are presenting yield problems.

4.6.1 THE TIMING SEQUENCE

Waveform observation uses a software routine that generates programming waveforms for the data stored in system RAM. An oscilloscope trigger pulse is generated every address increment. The oscilloscope trigger point reference is listed in Note 1 on the appropriate timing diagram. The address is automatically reset to Ø when the maximum PROM address is reached, and incrementing continues.

In the waveform observation procedure, fill the RAM with data so that it is possible to observe address-change waveforms, bit-to-program waveforms and no-bit-to program waveforms. In the procedure, take into account the output level of the PROM type (VOL or VOH) so that for either type of PROM a bit-to-program will appear on the same socket contact. The step-by-step procedure is described below.

4.6.2 THE TIMING DIAGRAMS

The manual contains a Timing Diagram for each PROM family. Each Timing Diagram contains a set of waveform

photographs that show critical programming parameters. The minimum and maximum parameter values are listed in the waveform variables table on the diagrams. Other voltage and time parameters are to be considered noncritical, with a tolerance of 10%.

For waveform photographs, the trigger was set at the leftmost graticule line; by taking into account any time-base variance, time comparisons can be made between photographs. (The time base is always the same for different waveforms in the same photographs.) Time base and volts-per-division settings are printed on each photograph.

The waveform names are called out on each photograph. (Waveform names correspond to the pin names on the Pinout Charts.) These charts tell which socket contact to probe when observing the waveforms.

Detailed photographs are included to magnify rapid voltage changes or particular pulses in a pulse train. In order to view these special conditions, it is necessary to use the delayed sweep feature on the oscilloscope. The number at the bottom of the photograph is the delay time for the pulse being viewed. The delayed Time/Division dial should be set to the time indicated at the top of the photograph. The Delay Viewer dial can then be used to bring into view the indicated sections of the signal tracers.

4.6.3 PROCEDURE

To observe waveforms, first follow the instructions for a complete calibration in paragraph 4.3. Then, complete the following steps:

a. Insert the Characterizer for the selected device.

b. Fill RAM with programming data. The correct data depends on the output polarity of the device. Pick the appropriate data in Table 4-1. The programmer manual will tell you how to fill RAM with the correct data.

Table 4-1. RAM Data for Waveform Observation

Output Polarity	Data
VOL	Hex 55
VOH	Hex AA

CAUTION

Remove all PROMs before entering calibration. DC calibration voltages, applied to the sockets before waveform generation, will damage any device in a socket. In order to observe waveforms with a PROM in the socket, use the normal programming mode.

c. Enter calibration at step 14 by following the instructions in the programmer manual.

d. To observe individual waveforms, as shown on a Timing Diagram, refer to the Pinout functions next to the Waveform Variable Table. The Pinout function illustration provides the numbers of the socket contacts to probe when observing the waveforms on the Timing Diagram.

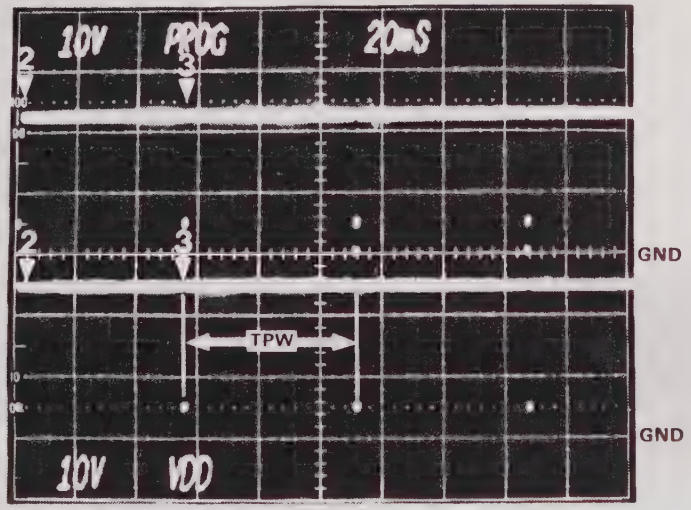
NOTE

Paragraph 4 explains considerations helpful in setting up and interpreting waveform displays.

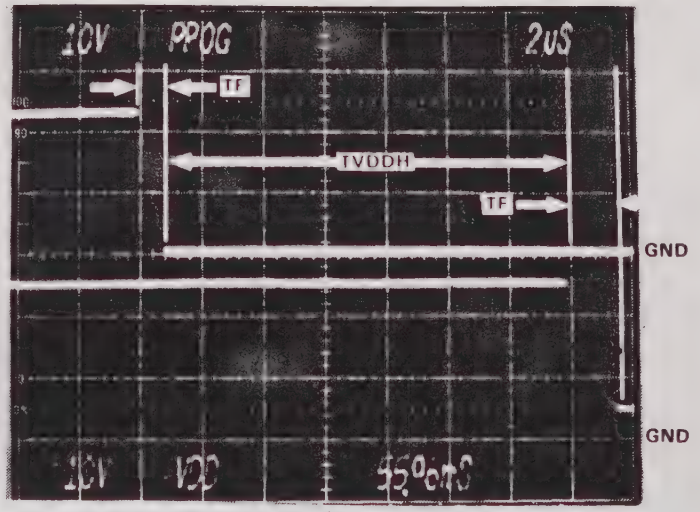
e. Exit the calibration mode as described in the appropriate programmer manual.

CAUTION

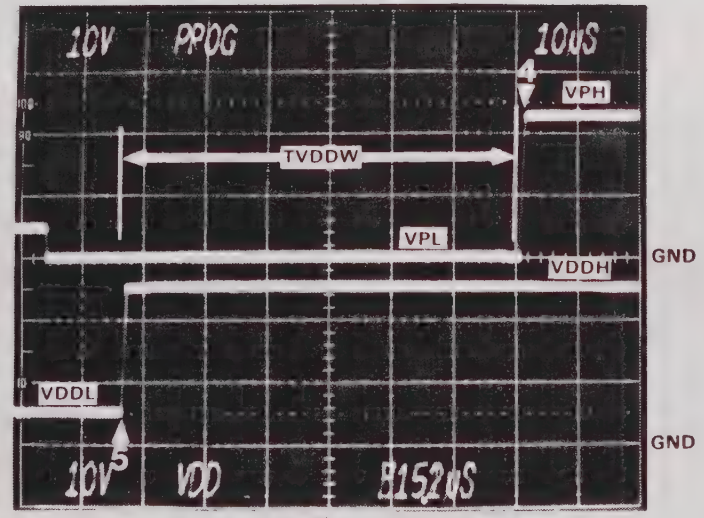
Exit calibration before attempting to program with the 40-Pin Gang Module.


10V PPOG 20mS
2
3
GND
TPW
GND
10V VDD

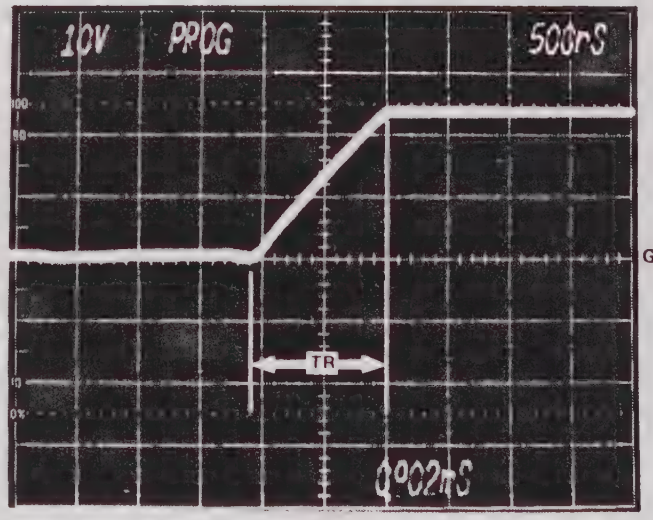
1


10V PPOG 2uS
TF
TVDDH
TF
GND
GND
10V VDD

3


10V PPOG 10uS
4
VPH
TVDDW
VPL
VDDH
GND
VDDL
GND
10V
5
VDD

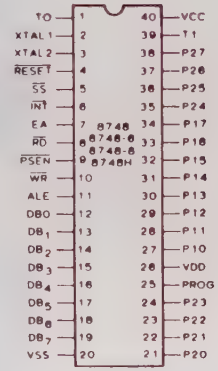
2


10V PPOG 500nS
GND
TR

4

NOTES

1. *Oscilloscope trigger point: Reset (Pin 4) of any Socket. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact (Pin 20) of any Socket.*
3. *The Pinout diagram, illustrated below, indicates which socket contact to probe to observe each waveform. To observe a bit-to-program waveform, use Pin 19 (D7/DB7) of any Socket. To observe a no-bit-to-program, use Pin 18 (D6/DB6) of any Socket.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *◄ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*



WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VDDH	24.0	25.0	26.0	V	
VEAH	21.5	23.0	24.5	V	Not Shown
VPH	21.5	23.0	24.5	V	
VDDL	4.75	5.00	5.25	V	
VEAL	–	–	5.25	V	Not Shown
VPL	–	–	0.2	V	
VCC	4.75	5.00	5.25	V	Not Shown
TPW	50	–	60	ms	
TCY	5.00	8.14	–	µs	Not Shown
TVDDW	4TCY	–	–	–	
TVDDH	Ø	–	–	µs	
TWW	4TCY	–	–	–	
TAW	4TCY	–	–	–	
TWA	4TCY	–	–	–	
TR	0.5	–	2.0	µs	
TF	0.5	–	2.0	µs	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	CF	RC	10/23/81
	B	ECN #4389		RC	11/23/81
	C	ECN #4413			
	D	ECN #4406			

DATA I/O ISSAQUAH, WA

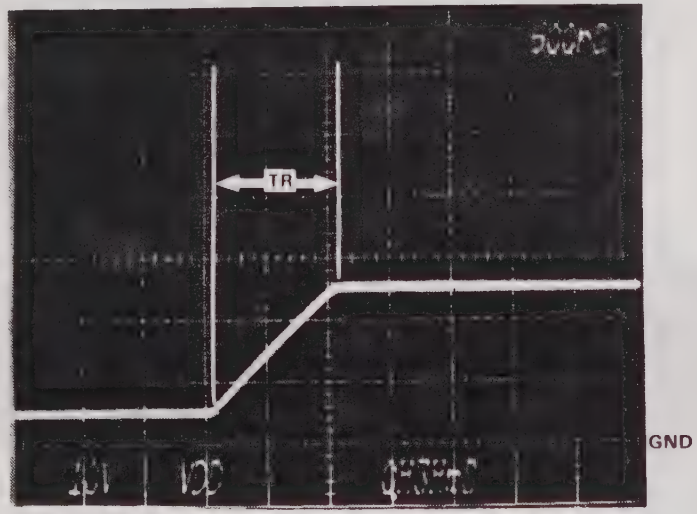
TITLE
TIMING DIAGRAM
8741A/8748

DRAWN BY: KJ

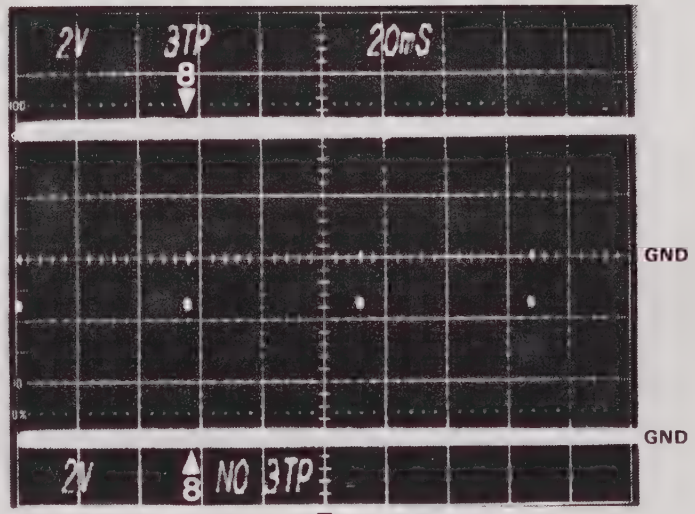
CHECKED BY: KH

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0073

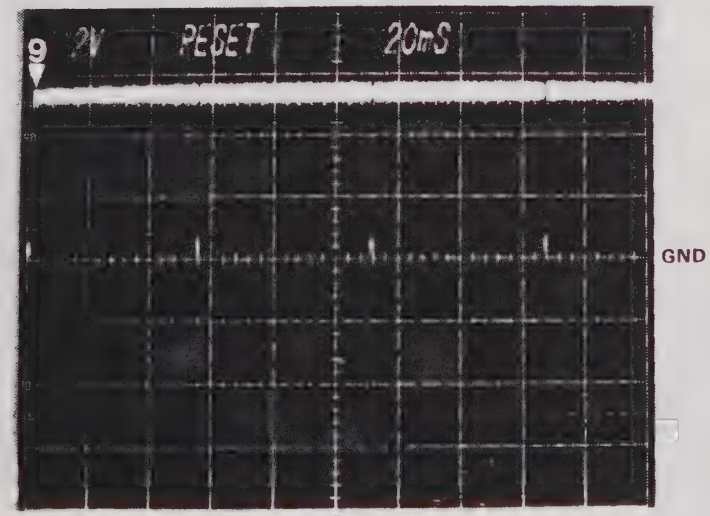
SCALE | SHEET 1/3


TR
GND

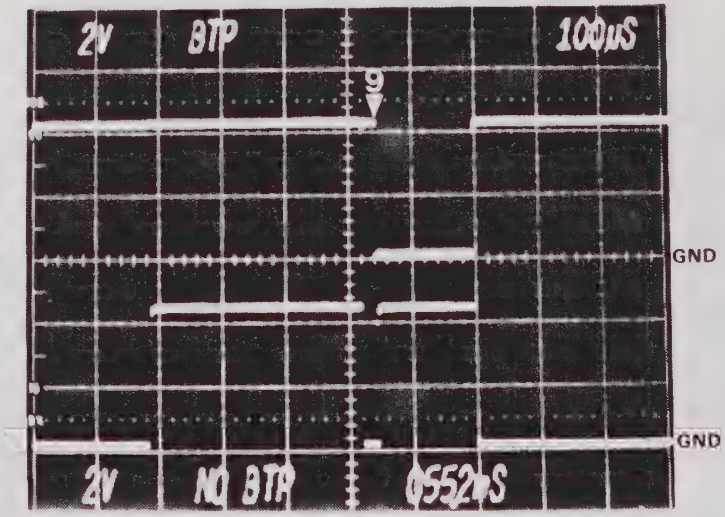
5


2V
3TP
8
20mS
GND
GND
2V
8
NO 3TP

7


9
2V
RESET
20mS
GND

6

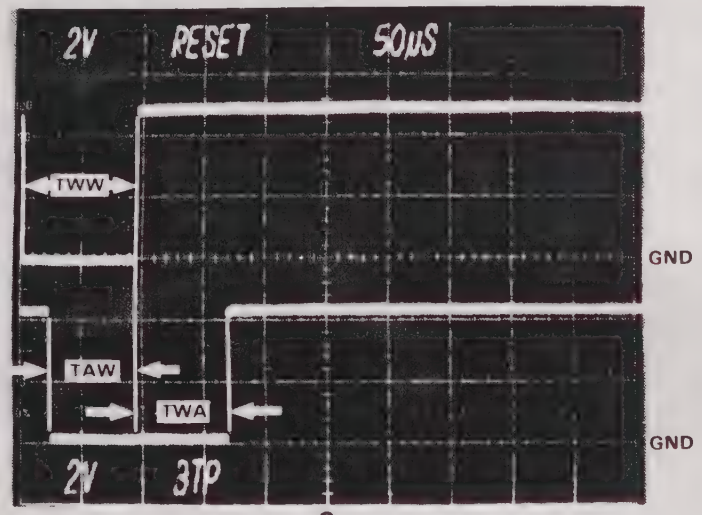

2V
BTP
100µS
9
GND
GND
2V
NO BTP

8

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1			

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM 8741A/8748		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0073
SCALE		SHEET 2/3

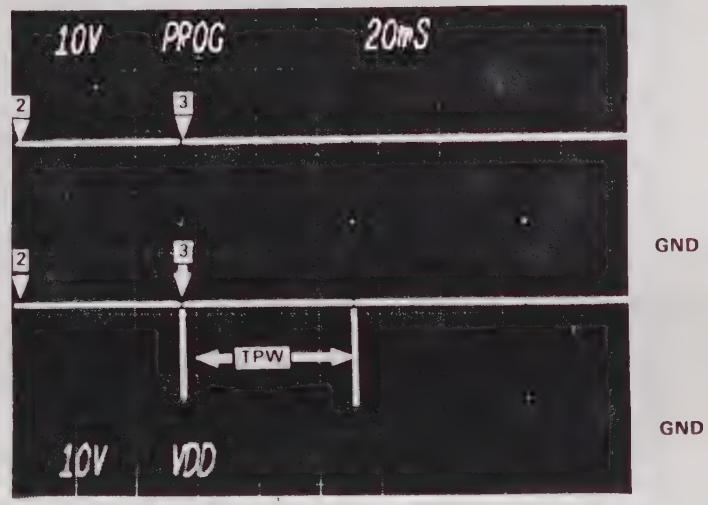


9

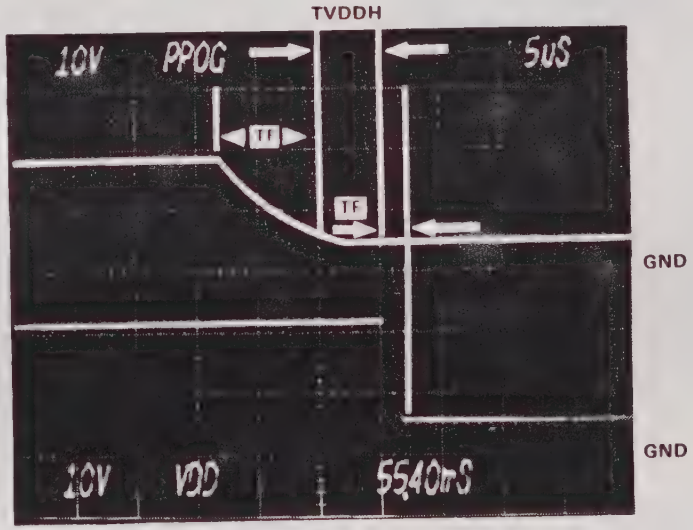
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1			

DATA I/O ISSAQUAH, WA

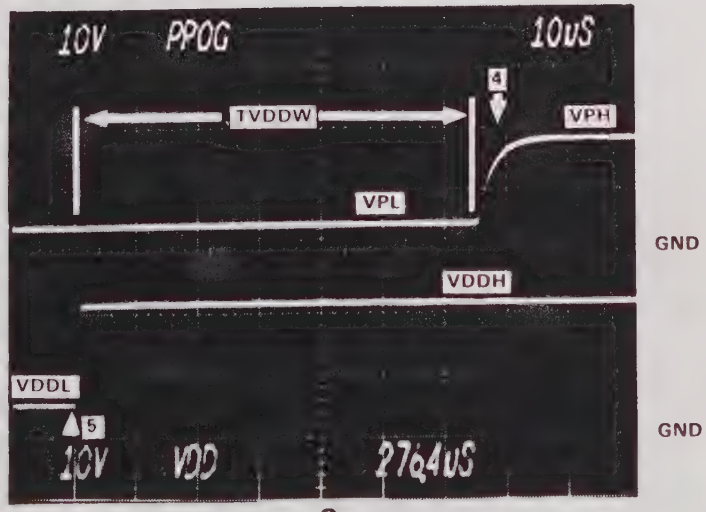
TITLE: TIMING DIAGRAM 8741A/8748		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0073
SCALE		SHEET 3/3


10V PPOG 20mS
2
3
2
3
TPW
GND
GND
10V VDD

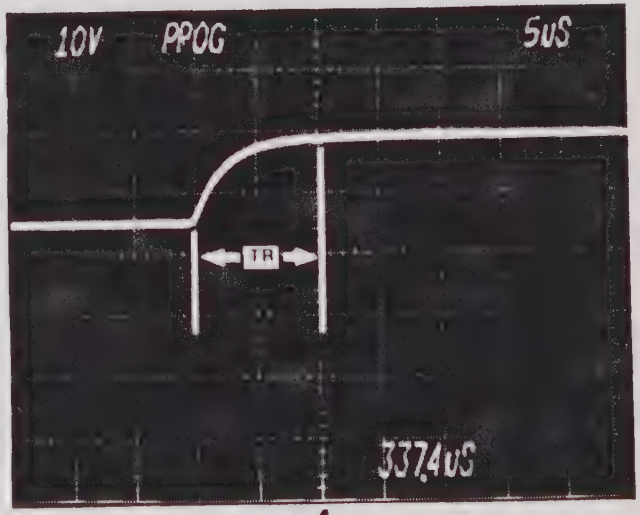
1


TVDDH
10V PPOG 5uS
TF
TF
GND
GND
10V VDD 5540mS

3


10V PPOG 10uS
4
TVDDW
VPH
VPL
GND
VDDH
VDDL
5
10V VDD 2764uS
GND

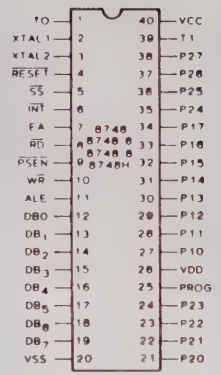
2

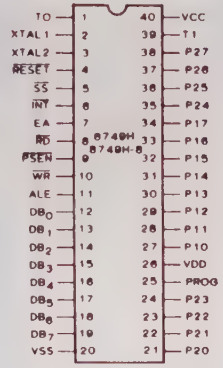

10V PPOG 5uS
TR
GND
3374uS

4

NOTES

1. *Oscilloscope trigger point: Reset (Pin 4) of any Socket. Trigger on the negative slope.*
2. *Oscilloscope ground reference: GND contact (Pin 20) of any Socket.*
3. *The Pinout diagram, illustrated below, indicates which socket contact to probe to observe each waveform. To observe a bit-to-program waveform, use Pin 19 (D7/DB7) of any Socket. To observe a no-bit-to-program, use Pin 18 (D6/DB6) of any Socket.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *◄ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*





WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VDDH	20.5	21.0	21.5	V	
VEAH	17.5	18.0	18.5	V	Not Shown
VPH	17.5	18.0	18.5	V	
VDDL	4.75	5.00	5.25	V	
VEAL	-	-	5.25	V	Not Shown
VPL	4.0	-	VCC	V	
VCC	4.75	5.00	5.25	V	Not Shown
TPW	50	-	60	ms	
TCY	4.0	4.19	15	us	Not Shown
TVDDW	Ø	-	1	ms	
TVDDH	Ø	-	1	ms	
TWW	4TCY	-	-	-	
TAW	4TCY	-	-	-	
TWA	4TCY	-	-	-	
TR	0.5	-	100	us	
TF	0.5	-	100	us	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE		RC	10/23/81
	B	ECN #4389		RC	11/23/81
	C	ECN #4413		RC	1/18/81
	D	ECN #4406		RC	2/10/82
	E	ECN #4607			6/21/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
8748H/8749H

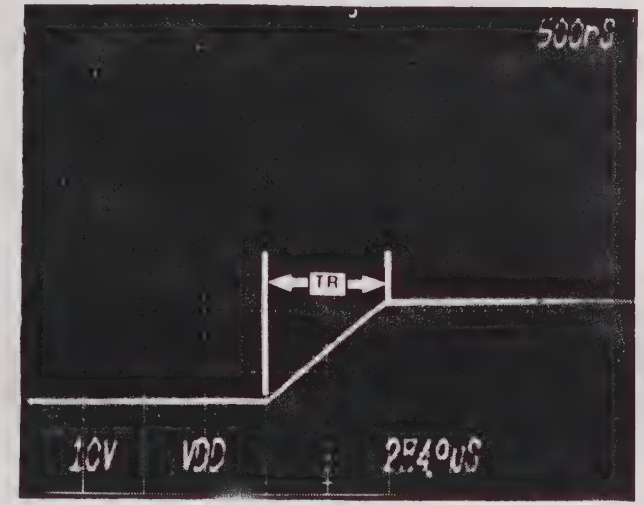
DRAWN BY: KJ

CHECKED BY: KH

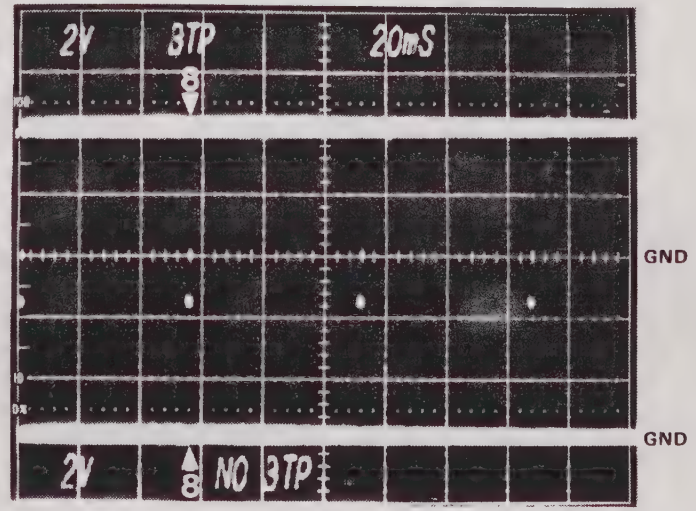
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0073

SCALE

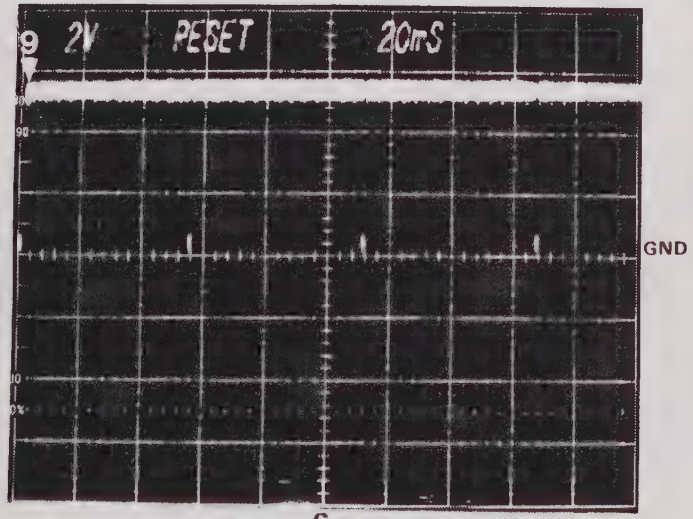
SHEET 1/3


500nS
TR
1CV
VDD
GND

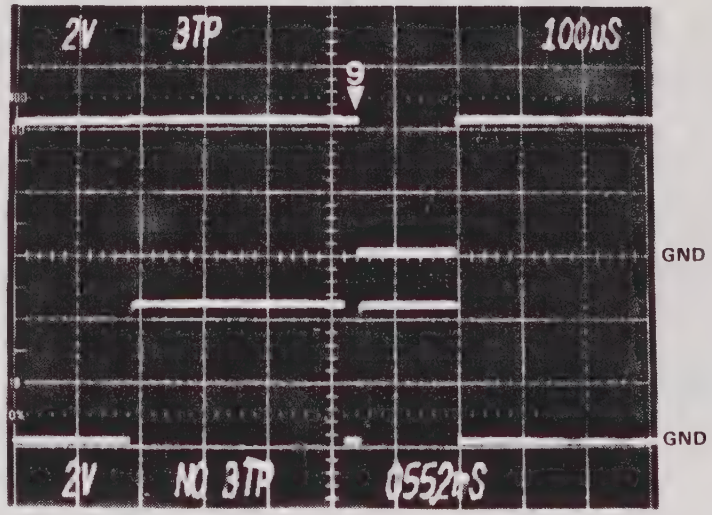
5


2V
3TP
20mS
GND
GND
2V
NO 3TP

7


2V
PESET
20mS
GND

6

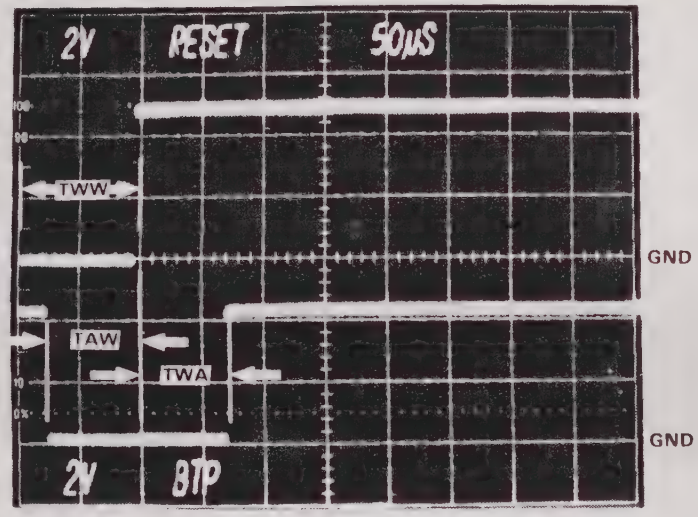

2V
3TP
100uS
GND
GND
2V
NO 3TP

8

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1			

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM 8748H/8749H		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0073
SCALE		SHEET 2/3



9

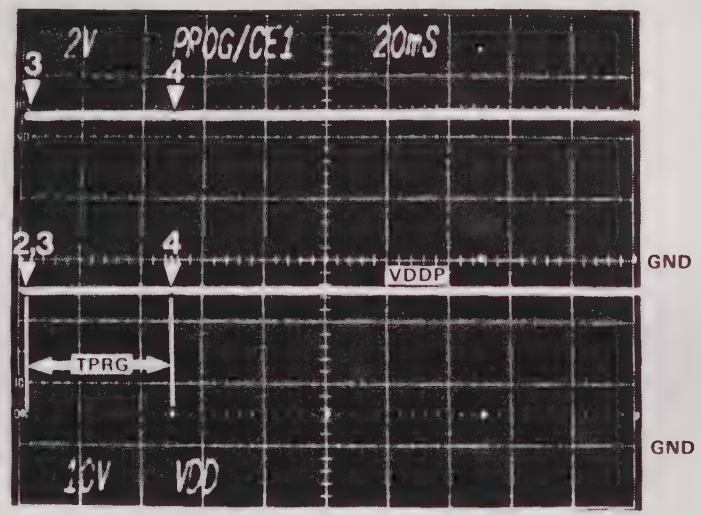
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1			

DATA I/O ISSAQUAH, WA

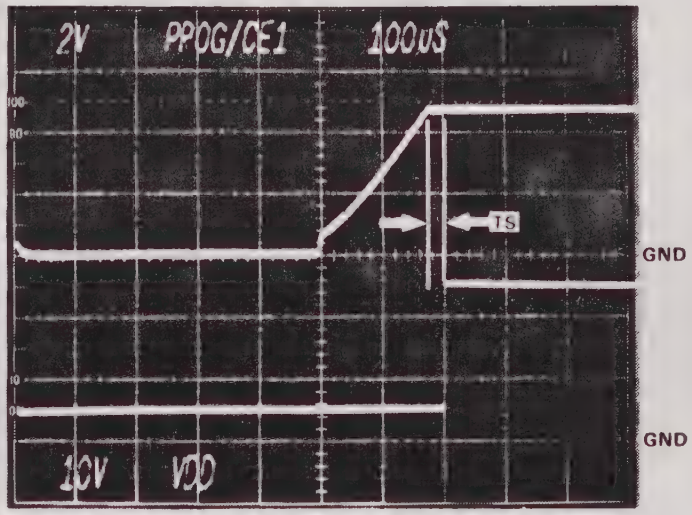
TITLE: TIMING DIAGRAM 8748H/8749H	DRAWN BY:
	CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0073

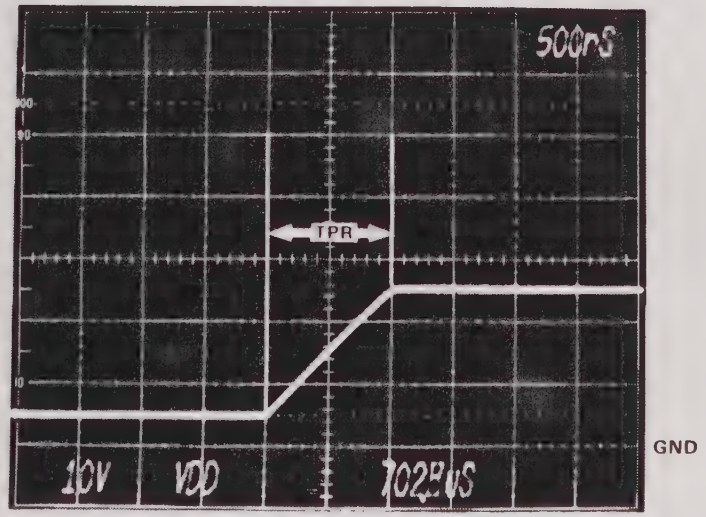
SCALE | SHEET 3/3


2V
PPOG/CE1
20mS
3
4
2,3
4
VDDP
GND
TPRG
GND
10V
VDD

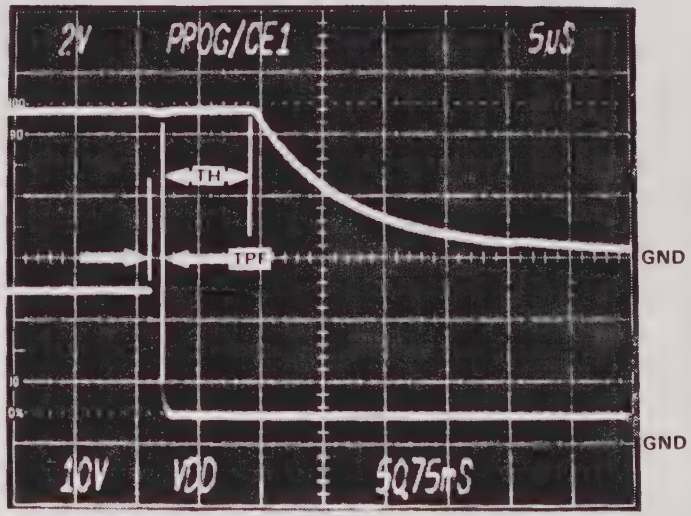
1


2V
PPOG/CE1
100uS
TS
GND
GND
10V
VDD

3


500nS
TPR
GND
10V
VDD
GND

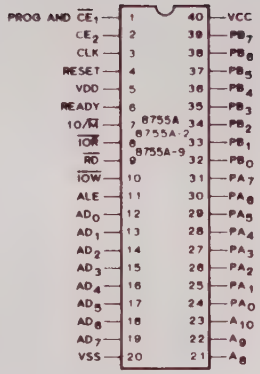
2


2V
PPOG/CE1
5uS
TH
TPF
GND
GND
10V
VDD

4

NOTES

1. *Oscilloscope trigger point: ALE (Pin 11) of any Socket. Trigger on the positive slope.*
2. *Oscilloscope ground reference: GND contact (Pin 20) of any Socket.*
3. *The Pinout diagram, illustrated below, indicates which socket contact to probe to observe each waveform. To observe a bit-to-program waveform, use Pin 19 (AD7) of any Socket. To observe a no-bit-to-program, use Pin 18 (AD6) of any Socket.*
4. *Time and voltage bases, as well as any delay times, are printed on each photograph. The time base is the same for all waveforms in a photograph.*
5. *◄ with a number indicates a waveform section expanded to show detail. The number refers to the detail photograph.*



WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VDDP	24.0	25.0	26.0	V	
VCC	4.75	5.00	5.25	V	Not Shown
TPRG	45	50	–	ms	
TS	2	–	–	µs	
TH	2	–	–	µs	
TPR	0.01	2.00	–	µs	
TPF	0.01	2.00	–	µs	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	CF	RC	10/23/81
	B	ECN #4389			
	C	ECN #4413			
	D	ECN #4406			

DATA I/O ISSAQUAH, WA

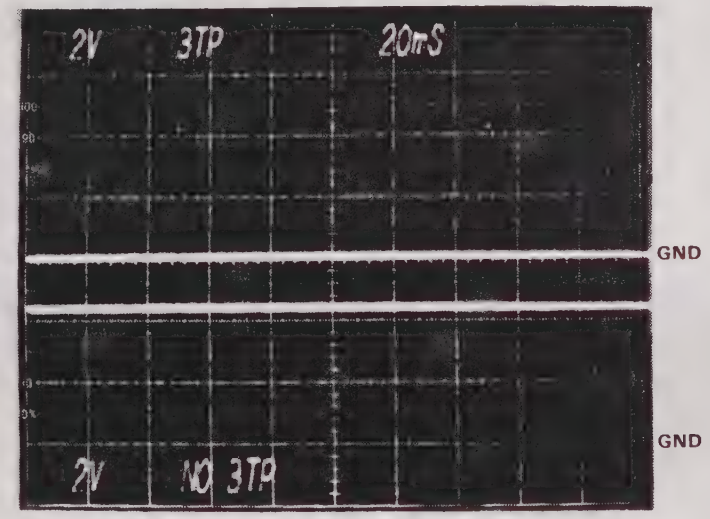
TITLE
TIMING DIAGRAM
8755A

DRAWN BY: KJ

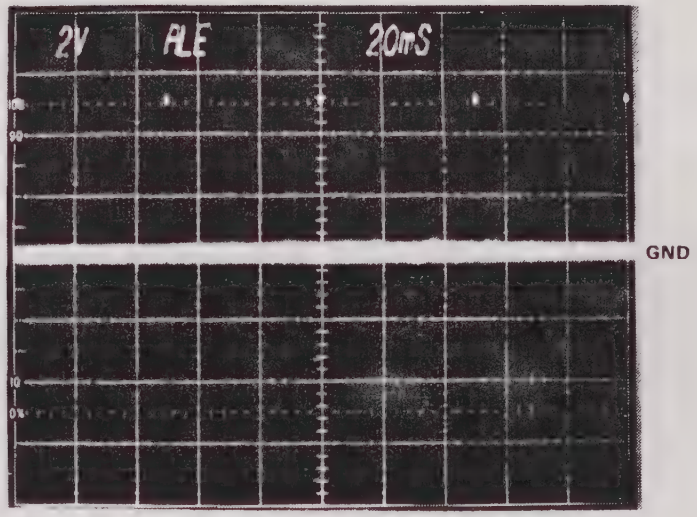
CHECKED BY: KH

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0073

SCALE | SHEET 1/2



5



6

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		See Sheet 1			

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM 8755A	DRAWN BY:
	CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0073

SCALE | SHEET 2/2

SECTION 5
MAINTENANCE

5.1 CLEANING

Inspect the Gang Module regularly, inside and out, for accumulated dirt or dust. Cleaning is easiest with a small, soft-bristle brush, or with a cotton-tipped swab for cramped areas.

Clean the Characterizer or accumulated dirt or dust on the edge connector could impede a good electrical contact. Clean the edge connector by gently rubbing the surface with a soft pencil eraser. No other maintenance of the Characterizer is required.

5.2 INSPECTION

Periodic inspection of the Gang Module can be a hedge against malfunction. A good time to schedule an inspection is before every calibration. Check cable connectors, card seating, socketed components, etc., for shorts, opens, or unstable continuity.

Particular care is required if heat-damaged components are found. It is important to find and correct the cause of overheating in order to prevent further damage.

Sockets require checking annually. Using an EPROM with a known data pattern, load data into RAM and make sure that it is transmitted faithfully to each socket by attempting to verify eight identically programmed devices, or the same device in each socket.

SECTION 6
TROUBLESHOOTING

6.1 INTRODUCTION

The following information is an aid to interpreting malfunctions and locating hardware failures in the Gang Module. System failures can be divided into two types:

a. No system operation

b. Persistent test errors

These categories, covered in paragraphs 6.2 and 6.3, will direct the service technician to the portion of the circuitry implicated by test errors or unacceptable calibration results. Table 6-1 can be used to isolate the problem to a suspect board or component. Section 7, *Circuit Description,* and Section 8, *Schematics,* provide additional information useful in troubleshooting.

After successful troubleshooting, perform a complete calibration of the Gang Module, as described in Section 4.

6.2 NO SYSTEM OPERATION

Perform the following steps if the system will not operate after installation of the Gang Module. After completing each step, determine whether the problem still exists.

a. Check for proper installation of the Gang Module (refer to Section 2).

b. Check all cables for proper insertion and orientation.

c. Check power supplies (refer to paragraph 4.4).

d. If steps a—c do not reveal the problem, contact your local Data I/O Service Center.

6.3 PERSISTENT OR INTERMITTENT TEST-STAGE ERRORS

Perform the following steps to isolate a system failure. After completing each step, determine whether the problem still exists.

a. Substitute a good device to determine if a hardware problem exists.

b. Check for proper installation of the Gang Module (refer to Section 2).

c. Check all cables for proper insertion and orientation.

d. Perform a complete calibration. Note any voltages still falling outside the indicated limits, and then refer to the corresponding test number in Table 6-1 to locate the suspect board or component. Referring to the circuit description (Section 7) and the schematics (Section 8) may also prove helpful.

e. Check that the Characterizer is properly inserted in its socket. If the error persists, examine the edge connector on the Characterizer; if it is dirty, clean it according to the procedure in Section 5. If a) the error is isolated to the Characterizer, and b) the edge connector is clean and mates properly with its socket, the Characterizer must be replaced.

f. If steps a—e do not reveal the problem, contact your local Data I/O Service Center.

Table 6-1. Troubleshooting the Circuitry

TEST NO.	SUSPECT BOARD(S)	SUSPECT COMPONENTS
1	701-1474-001, 701-1766-001	—
2	701-1474-001	Q10
3	702-1937-001	U9, DS1-8
4	701-1474-001	Q4, Q12, U4, Q8
5	701-1474-001	U3, Q23, Q26, Q27
6	701-1474-001	Q8, Q9, U4
7	701-1474-001	Q17, Q18, VR2
8	701-1474-001	U2
9	702-1937-001	U9
10	701-1474-001	Q4, Q12, U4, Q8
11	701-1474-001	U3, Q23, Q26, Q27
12	701-1474-001	Q8, Q9, U4
13	701-1474-001	U2, CR1
14	701-1474-001	Q5, VR1
15	701-1474-001	U3, Q23, Q26, Q27
16	701-1474-001	Q10, CR8
17	701-1766-001	U3, U5, U6
18	701-1766-001	U3, U5, U6
19	701-1766-001	U3, U5, U6
20	701-1766-001	U3, U5, U6
21	701-1766-001	U5, U6
22	701-1766-001	U5, U6
23	701-1766-001	U5, U6
24	701-1766-001	U5, U6
25	701-1766-001	U1, U9
26	701-1766-001	U1, U9
27	701-1766-001	U1, U9
28	701-1766-001	U1, U9
29	701-1766-001	U1, U9
30	701-1766-001	U1, U9
31	701-1766-001	U1, U9
32	701-1766-001	U1, U9
33	701-1766-001	U1, U9

SECTION 7
CIRCUIT DESCRIPTION

7.1 INTRODUCTION

This section defines the functions of the Gang Module's principal hardware components. Each circuit card is explained by a block diagram and a written description.

7.2 GENERAL ARCHITECTURE

7.2.1 THE LINK BETWEEN THE GANG MODULE AND THE PROGRAMMER

The Gang Module is controlled by the programmer's processor through the Gang Module's mating connector. Pin functions of the processor bus are shown in Table 7-1.

The control software for the Gang Module is located in PROM on the Analog Control Card.

7.2.2 THE BUSES

The programmer's address bus, data bus, R/$\overline{W}$ line and $\overline{V \bullet \emptyset_2}$ line control the gates and registers on the Waveform Generator and Analog Control Cards. The device bus gathers the programming waveforms produced by these cards and transmits them to the Gang Socket Adapter. Figure 7-1 shows the relationships among the buses.

7.3 COMPONENT LAYOUT

Figure 7-2 shows the component layout of the Gang Module. The principal components are described in paragraphs 7.3.1—7.3.5.

7.3.1 MOTHERBOARD

The motherboard accepts the signals and power supplies from the programmer and transmits them to two identical 72-pin connectors. See Figure 7-3.

7.3.2 WAVEFORM GENERATOR

The waveform generator provides all signals, in addition to the addresses and data required, for programming

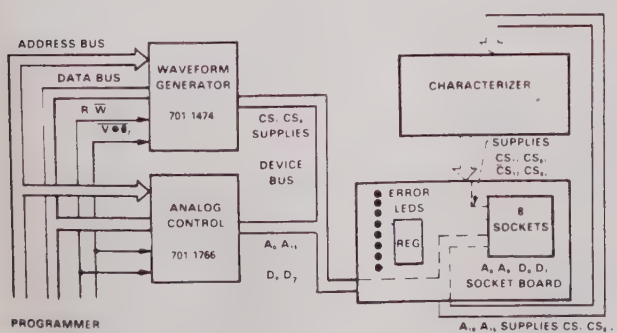


Figure 7-1. Block Diagram, Gang Module Electronics

Table 7-1. Pin Functions, Programmer's Extended Processor Bus (at J2 and J3)

Pin	Function		Pin	Function	
1	A_0	Processor Address	A	A_5	Processor Address
2	A_1		B	A_6	
3	A_2		C	A_7	
4	A_3		D	A_8	
5	A_4		E	A_9	
6	A_{10}		F	A_{11}	
7	A_{12}		H	A_{13}	
8	A_{14}		J	A_{15}	
9	DO_1	Processor Data Bus	K	DI_1	Control Register
10	DO_2		L	DI_2	
11	DO_3		M	DI_3	
12	DO_4		N	DI_4	
13	DO_5		P	DI_5	
14	DO_6		R	DI_6	
15	DO_7		S	DI_7	
16	DO_8		T	DI_8	
17	Ver. A	Control	U	Ver. B	Control
18	Start		V	Clk. Inh.	
19	W/L		W	"26"	
20	VOL/VOH		X	"36"	
21	+5V	Power	Y	-9V	Power
22	+Prog.		Z	+24V	
23	Gnd.		AA	-5V	
24	Sense		BB	Operate	
25	+48V		CC	Unreg. H.V.	
26	Gnd.		DD	Gnd.	
27	Spare		EE	Spare	
28	Spare		FF	Spare	
29	Spare		HH	Spare	
30	$\overline{IRQ}$	Processor Control	JJ	Gate Enable	Port Control
31	R/$\overline{W}$		KK	Extend	
32	$\overline{V \bullet \emptyset_2}$		LL	+18V Raw	
33	Interlock	Port Control	MM	PP	Control
34	+10V Raw		NN	RR	
35	$\overline{Write}$	Control	PP	Read	
36	$\overline{R}$		RR	Fwd.	

devices. These signals are generated by the blocks shown in Figure 7-4.

The V_{CC} supply uses a TL 430 shunt regulator (VR2) a series pass transistor (Q18) and remote sensing to develop +5 V at the socket. It has a current-sense resistor (R55) and transistor (Q19) which can set the over-current memory in case of a short circuit.

In order to provide the large number of voltage levels required for the program pulse, a DA-controlled V_{PP} supply is used. This supply consists of differential pair, Q13/15 and Q14/16 driving a current source, Q6, and an emitter

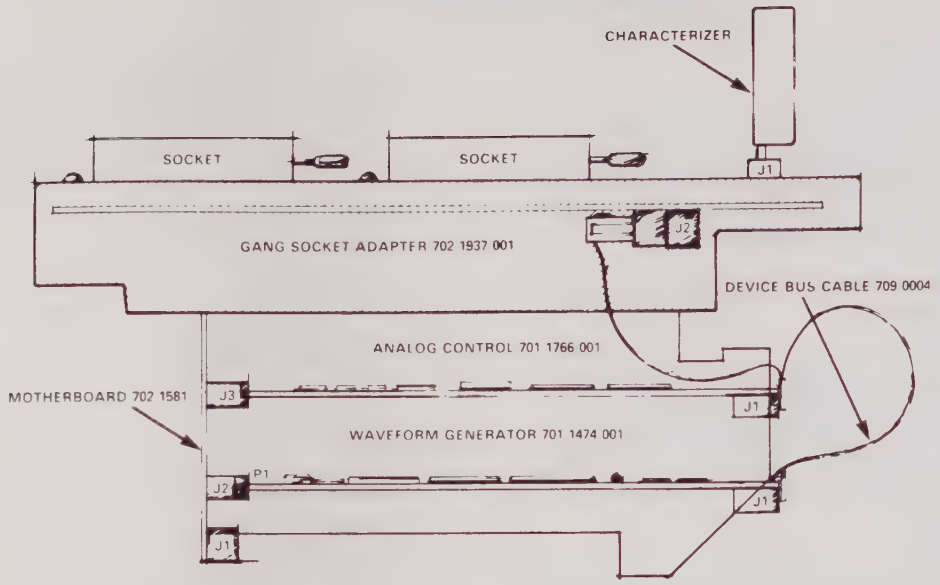


Figure 7-2. Principal Components of the Gang Module

follower, Q8. The noninverting input of the differential pair is grounded; the inverting input is connected to the output current sink of the D-A converter. The value of R33 determines the voltage gain of the supply. The digital input to the D-A converter is stored in the DAC register, U5.

The program-pulse switch uses the V_{PP} supply to generate program pulses with controlled rise and fall times. Capacitors C4 and C5 control the rise time and capacitor C6 controls the fall time. Program pulse floats at about +5 volts when not preparing or actively programming.

The V_{DD} programming voltage circuit consists of two parts: the V_{DD} switch and the V_{DD} supply. The V_{DD} switch selects either the V_{PP} supply voltage, the V_{DD} supply voltage or zero volts (ground level.)

The V_{DD} supply uses a TL 430 shunt regulator (VR1) and a series pass transistor (Q5) to develop +5 volts. It is diode protected from the V_{PP} supply by CR6. It also has a current-sense resistor (R8) and transistor (Q1) which can set the over-current memory in case of a short circuit.

When the V_{DD} switch selects or deselects V_{PP}, the rise and fall times are controlled by capacitor C7.

The CS supply is a low-current, multilevel supply for the CS-buffer pullup resistors. A TL430 shunt regulator (VR3) driving a current source and two pots (R37, R38) provides three selectable levels.

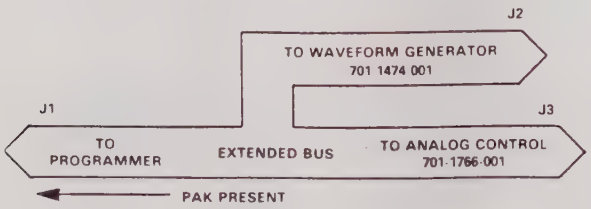


Figure 7-3. Block Diagram, Motherboard

The CS register (U6) drives one CS open-collector buffer. The buffer consists of a Darlington transistor (Q26) connected in parallel with an ordinary transistor (Q27). The ordinary transistor provides a low saturation voltage, and the Darlington transistor can sink large currents that would occur from a shorted device being programmed.

The overcurrent memory is set when V_{CC}, V_{DD} or V_{PP} supplies reach an overcurrent condition, shutting off the supplies. The state of the overcurrent memory is sensed by a line connecting the memory to the programmer's internal status register. This information is used by the programmer to detect shorted devices.

The device pull-up circuit (U1) provides the necessary signals to drive the device-backward test circuitry on the Socket Driver Board.

The crystal oscillator (Y1) provides a 3.579545 MHZ squarewave for use while programming or reading the UPI-41 or MCS-48 family of devices.

7.3.3 ANALOG CONTROL CARD

The Analog Control Card (P/N 701-1766) is shown in block-diagram form in Figure 7-5. PROMs U7 and U8 which store the Gang Module software are contained on the Analog Control Card. These PROMs connect to the extended address bus directly, and to the data bus through bidirectional buffer U14. An additional 128 bytes of scratch-pad RAM (U12) are connected to the extended processor bus. Regulator Q1 is the 12-volt source for the 2708 or 2716 PROMs.

Three PROMs (U10, U11, and U15) on the card develop decode signals. The eight high-order address lines address a 256x4 PROM (U11). Four outputs of this PROM drive four inputs of a 32x8 PROM (U15). R/$\overline{W}$ is fed to the fourth

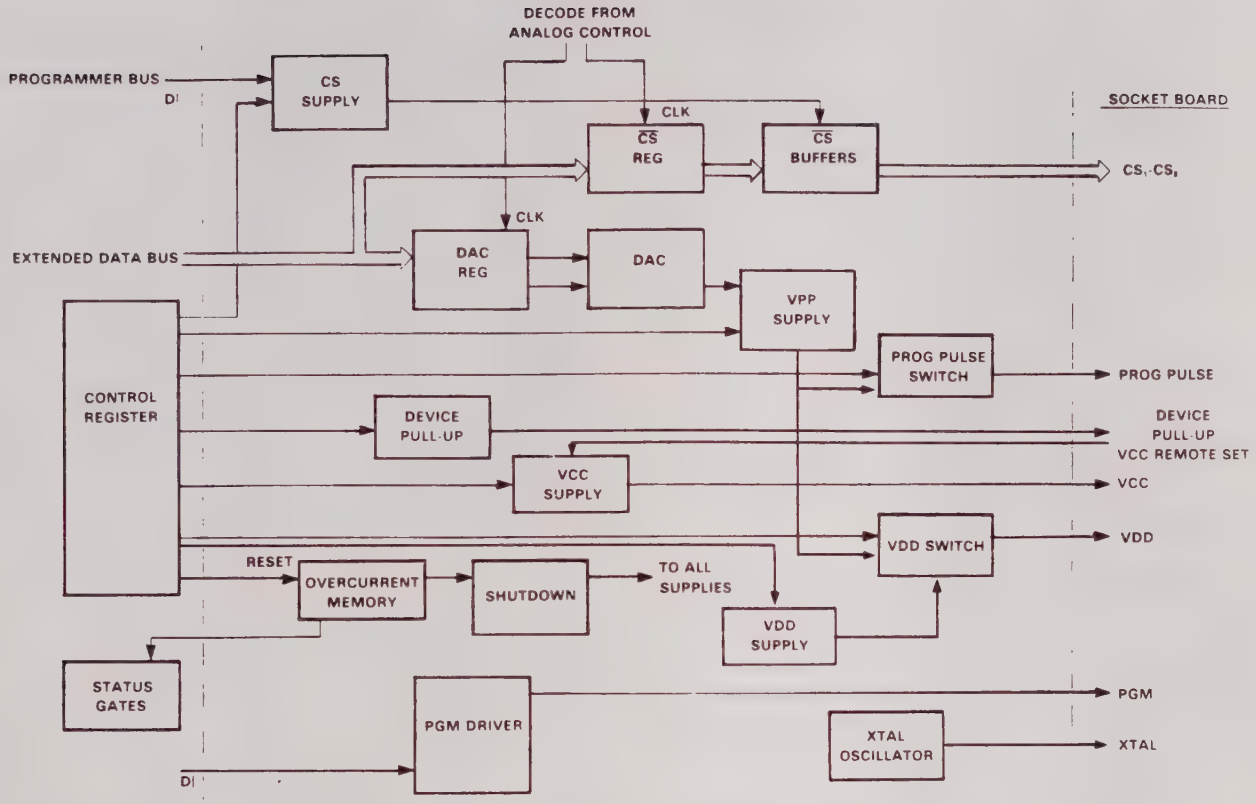


Figure 7-4. Block Diagram, Waveform Generator

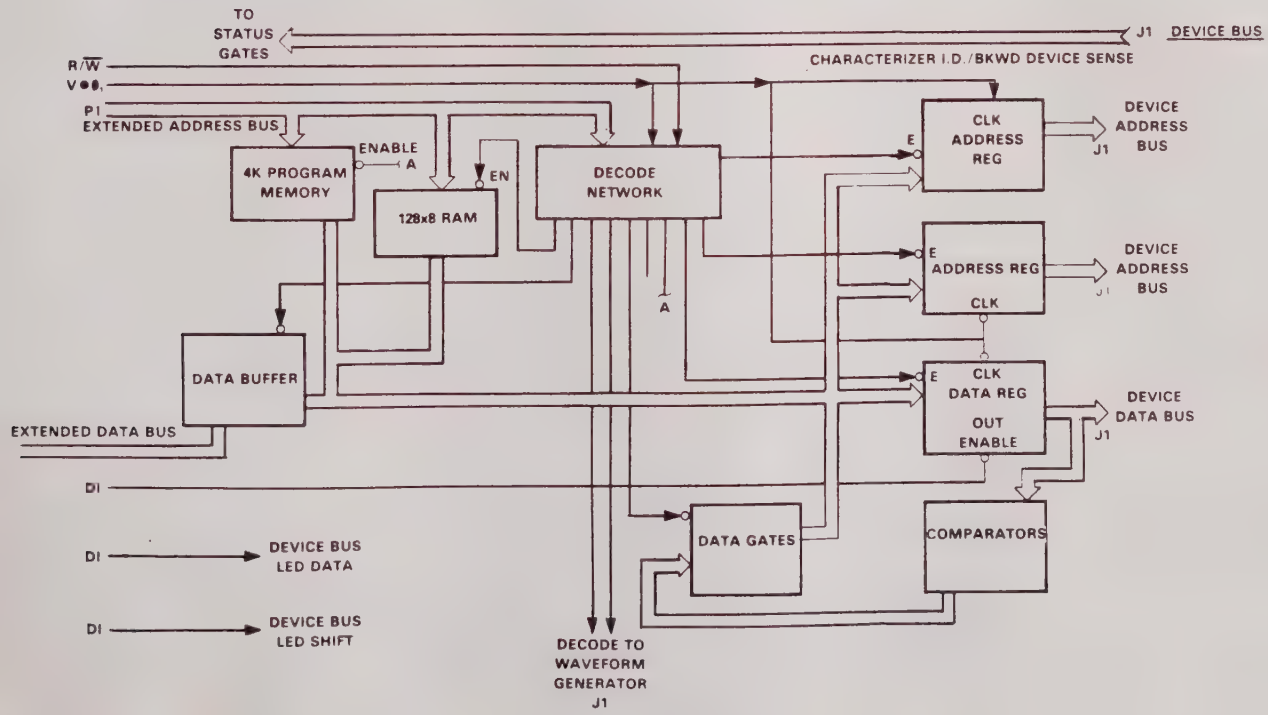


Figure 7-5. Block Diagram, Analog Control Card

input and $V \bullet \emptyset_2$ is fed to the CS line. The resulting signals from U15 are timed to decode the software PROMs, RAM and data buffer (U14) and to provide the required gate-enable signal to the programmer.

The fourth output of U11 is connected to one input of another 32x8 PROM, U10. R/W and three address lines, A_7, A_6 and A_5, are the remaining inputs to U10. U6 is selected by $\overline{V \bullet \emptyset_2}$, with the resulting outputs from U6 providing the decode signals for the various control registers and gates, each of which occupies 32 addresses.

The device address and data drivers consist of six 74LS173 registers driving the device bus. The card includes 10K pullups to guarantee that the lines will pull above +3 V, a requirement for some devices. Overvoltage protection is provided on each line by a 5.1 V zener. The address drivers are enabled permanently; the data drivers can be enabled by DI_3. Device data is read and strobed to the bus by a 74LS244 buffer (U4).

Table 7-2 gives the pin functions of the device bus.

Table 7-2. Pin Functions, Device Bus (at J1)

Pin	Function	Pin	Function
14	P_{A0}	32	VCC
16	P_{A1}	28	VDD
17	P_{A2}	49	Device Pull-up
18	P_{A3}	48	XTAL
19	P_{A4}	47	Prog. Pulse
20	P_{A5}	46	Pgm.
21	P_{A6}	1	ID0
22	P_{A7}	2	ID1
23	P_{A8}	50	ID2
24	P_{A9}	15	ID3
36	P_{A10}	26	Bkwd Device Sense
37	P_{A11}	27	Data
40	P_{A12}	25	Clk
41	P_{A13}	11	+5 V
42	P_{A14}	13,38, 39	Gnd.
43	P_{A15}	35	PCS_1
5	P_{D1}	34	PCS_2
4	P_{D2}	33	PCS_3
3	P_{D3}	44	PCS_4
8	P_{D4}	31	PCS_5
7	P_{D5}	30	PCS_6
6	P_{D6}	29	PCS_7
9	P_{D7}	45	PCS_8
10	P_{D8}	12	VCC Sense

7.3.4 GANG SOCKET BOARD

The Gang Socket Board distributes to the device sockets the signals developed on the Analog Control Card and the Waveform Generator Card. Refer to the Block Diagram, Figure 7-6. The low-order address and data lines go directly to the device sockets, as these lines are the same for all devices. The supply lines, high-order address lines, and chip selects go to the Characterizer and then to the device sockets.

Four I.D. lines from the Characterizer are connected, via the Analog Control Card, to status gate inputs of the programmer. The eight socket LEDs on the Gang Module

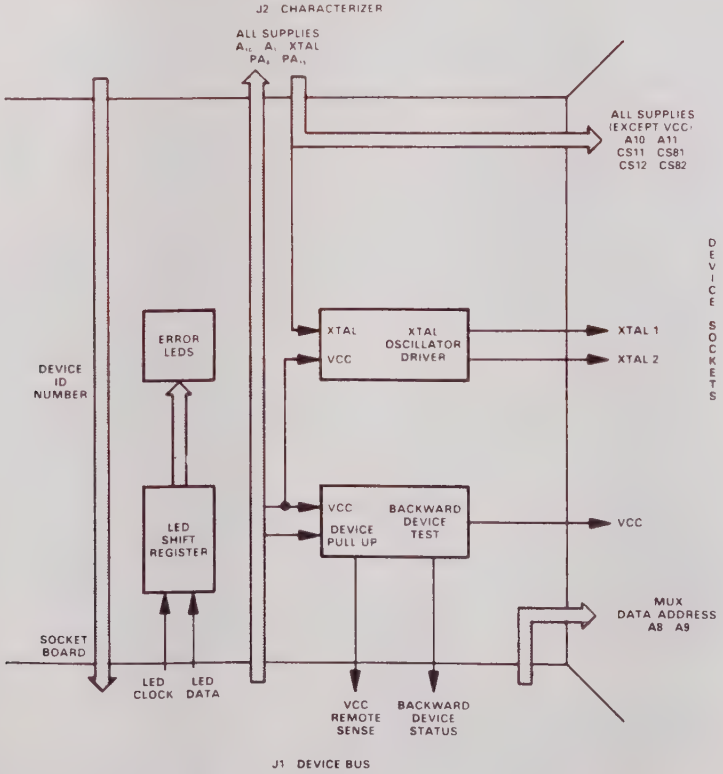


Figure 7-6. Block Diagram, Gang Socket Board

are driven by shift register U9. The clock and data lines originate at the programmer's data register (U40), and the signals from these lines arrive via the Analog Control Card.

The crystal oscillator driver (U10) provides the XTAL 1 and XTAL 2 signals for programming the UP1-41 and MCS-48 microcomputers. It receives its input signal through the Characterizer from the crystal oscillator (Y1) on the Waveform Generator. It is enabled only when Vcc is on.

The device-backward test circuitry is connected to each socket's Vcc pin. When Vcc is high, it is applied to all sockets through eight diodes; remote sensing of the voltage at the master socket is provided.

When Vcc is brought to zero, the socket Vcc lines can be pulled up by the Vcc pull-up (Q2) through eight 27 ohm resistors. The voltage at each socket is compared with a reference voltage by comparators U11 and U12. The outputs of the comparator are "ANDed" so that if any device is in backwards it will force the device-backward status line low.

Vcc is capacitively coupled to ground at each socket to absorb inductive spikes.

7.3.5 CHARACTERIZERS

The Characterizers manipulate the supplies, high-order address lines and chip selects to adapt the Gang Module to many devices. See the block diagram in Figure 7-7.

Each Characterizer contains four I.D. jumpers, which are read by the Gang Module to determine the type of device to be programmed. Also contained in the Characterizers is circuitry which configures the pinout of the Gang Module to each particular device to be programmed.

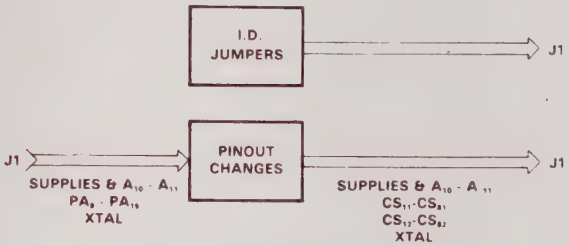
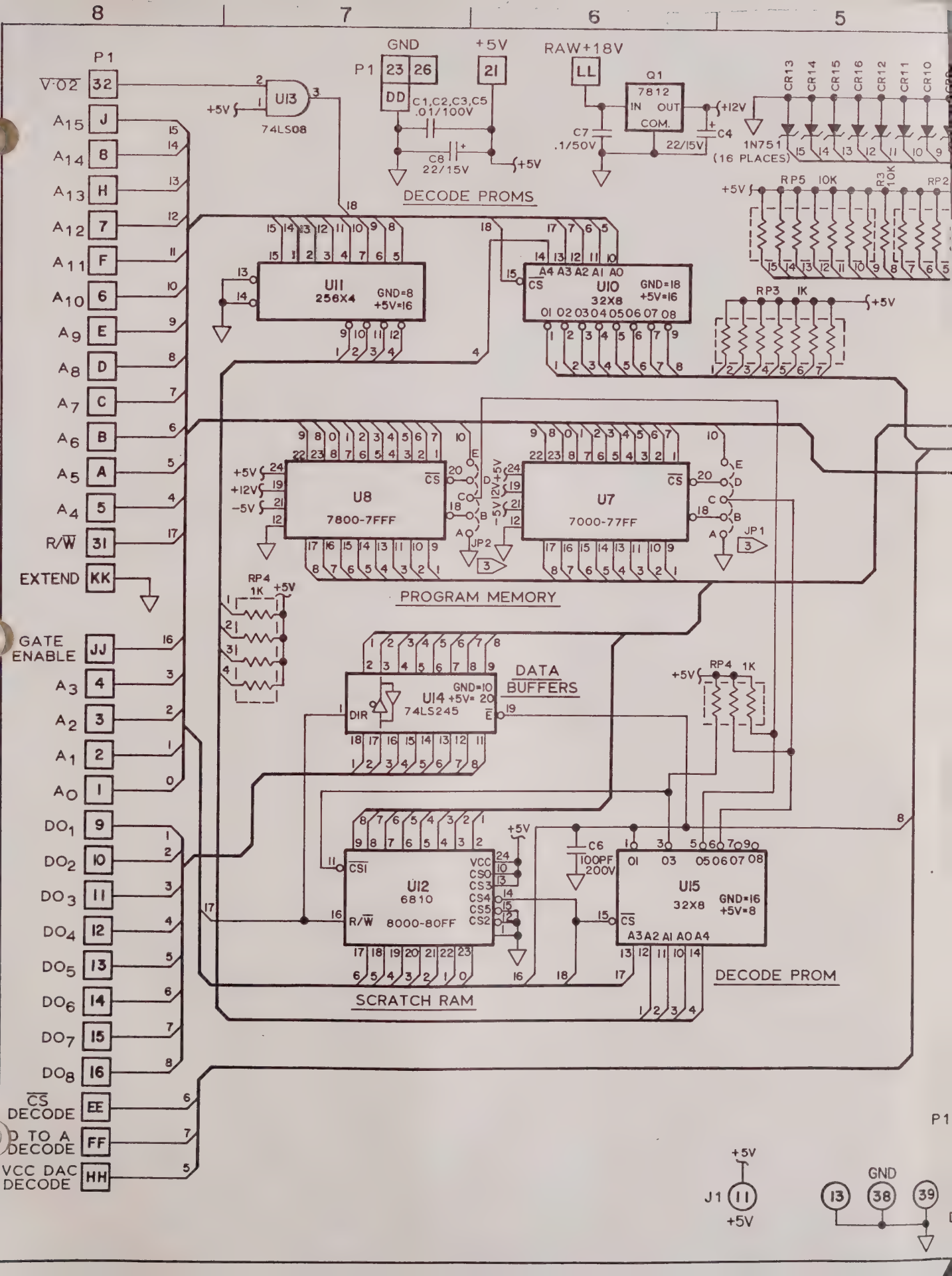


Figure 7-7. Block Diagram, Characterizer

SECTION 8
SCHEMATICS

The schematics are in this order:

Gang Module Analog Control	30-701-1766
Gang Module Waveform Generator (2 pages)	30-701-1474
40-Pin Gang Socket Board (2 pages)	30-702-1937
CPU-Controlled Pak Motherboard	008-1999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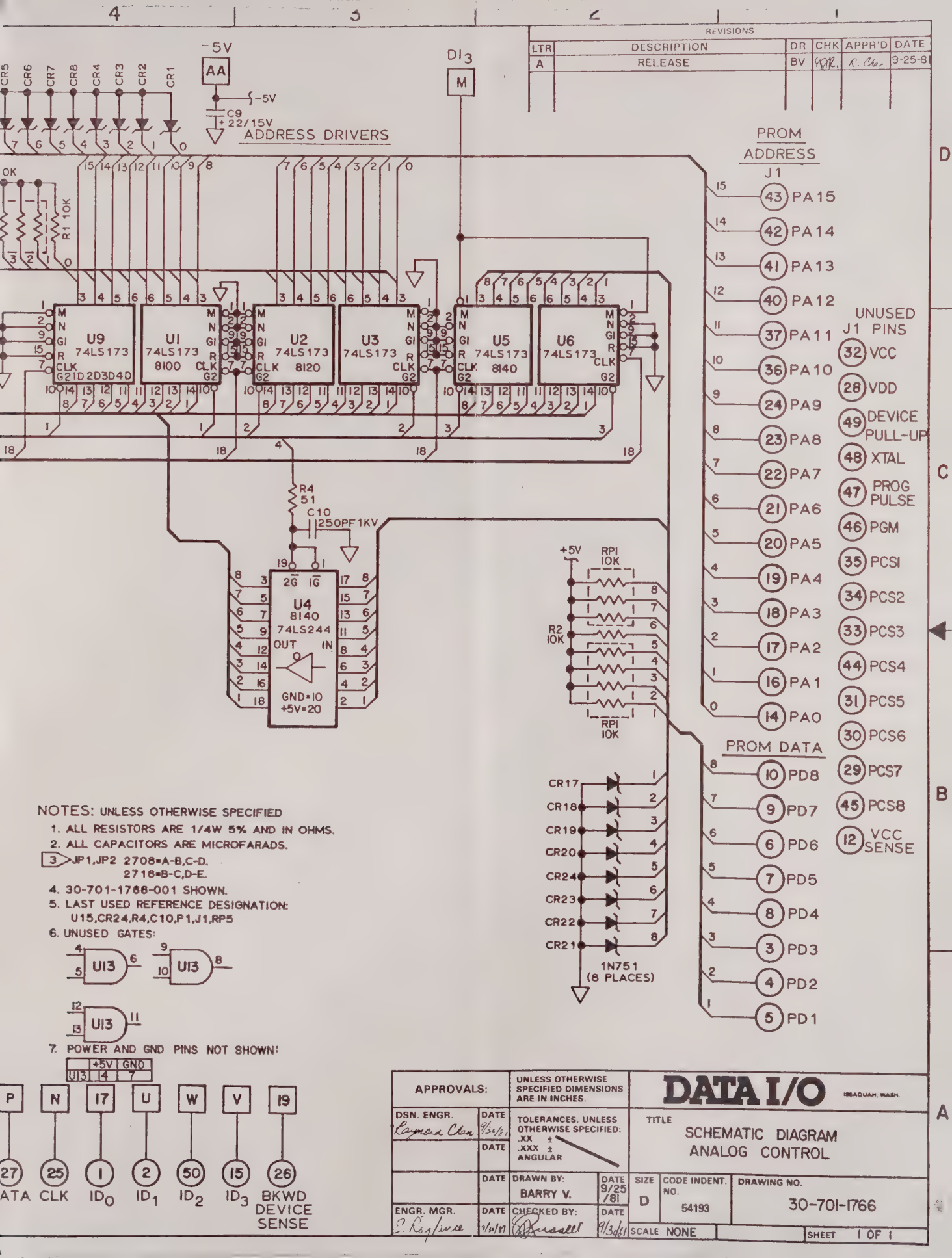
7
6
5
P1
V-02
32
A15
J
A14
B
A13
H
A12
7
A11
F
A10
6
A9
E
A8
D
A7
C
A6
B
A5
A
A4
5
R/W
31
EXTEND
KK
GATE ENABLE
JJ
A3
4
A2
3
A1
2
A0
1
DO1
9
DO2
10
DO3
11
DO4
12
DO5
13
DO6
14
DO7
15
DO8
16
CS DECODE
EE
D TO A DECODE
FF
VCC DAC DECODE
HH
U13
74LS08
+5V
GND
P1
23
26
DD
21
C1,C2,C3,C5
.01/100V
C8
22/15V
DECODE PROMS
RAW+18V
LL
Q1
7812
IN
OUT
COM.
C7
.1/50V
22/15V
C4
+12V
CR13
CR14
CR15
CR16
CR12
CR11
CR10
1N751
(16 PLACES)
RP5
10K
R3
10K
RP2
RP3
1K
U11
256X4
GND=8
+5V=16
U10
32X8
A4 A3 A2 A1 A0
CS
O1 O2 O3 O4 O5 O6 O7 O8
GND=18
+5V=16
U8
7800-7FFF
U7
7000-77FF
JP1
JP2
PROGRAM MEMORY
RP4
1K
DATA BUFFERS
U14
74LS245
DIR
GND=10
+5V=20
U12
6810
8000-80FF
CS1
R/W
VCC
CS0
CS3
CS4
CS5
CS2
SCRATCH RAM
C6
100PF
200V
U15
32X8
GND=16
+5V=8
A3 A2 A1 A0 A4
DECODE PROM
J1
11
13
38
39
GND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ADDRESS DRIVERS
PROM ADDRESS
J1
PA15 PA14 PA13 PA12 PA11 PA10 PA9 PA8 PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0
UNUSED J1 PINS
VCC VDD DEVICE PULL-UP XTAL PROG PULSE PGM PCS1 PCS2 PCS3 PCS4 PCS5 PCS6 PCS7 PCS8 VCC SENSE
PROM DATA
PD8 PD7 PD6 PD5 PD4 PD3 PD2 PD1
U9 74LS173
U1 74LS173 8100
U2 74LS173 8120
U3 74LS173
U5 74LS173 8140
U6 74LS173
U4 8140 74LS244
R1 10K
R2 10K
R4 51
C10 250PF 1KV
C9 22/15V
RPI 10K
CR17 CR18 CR19 CR20 CR24 CR23 CR22 CR21
1N751 (8 PLACES)
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W 5% AND IN OHMS.
2. ALL CAPACITORS ARE MICROFARADS.
3. JP1,JP2 2708=A-B,C-D. 2716=B-C,D-E.
4. 30-701-1766-001 SHOWN.
5. LAST USED REFERENCE DESIGNATION: U15,CR24,R4,C10,P1,J1,RP5
6. UNUSED GATES:
7. POWER AND GND PINS NOT SHOWN:
P N 17 U W V 19
27 25 1 2 50 15 26
ATA CLK ID0 ID1 ID2 ID3 BKWD DEVICE SENSE
APPROVALS:
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DSN. ENGR. Raymond Chan 9/24/81
TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR
DRAWN BY: BARRY V. 9/25/81
ENGR. MGR. C. Roylance 9/24/81
CHECKED BY: Russell 9/30/81
DATA I/O ISSAQUAH, WASH.
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DRAWING NO. 30-701-1766
SCALE NONE
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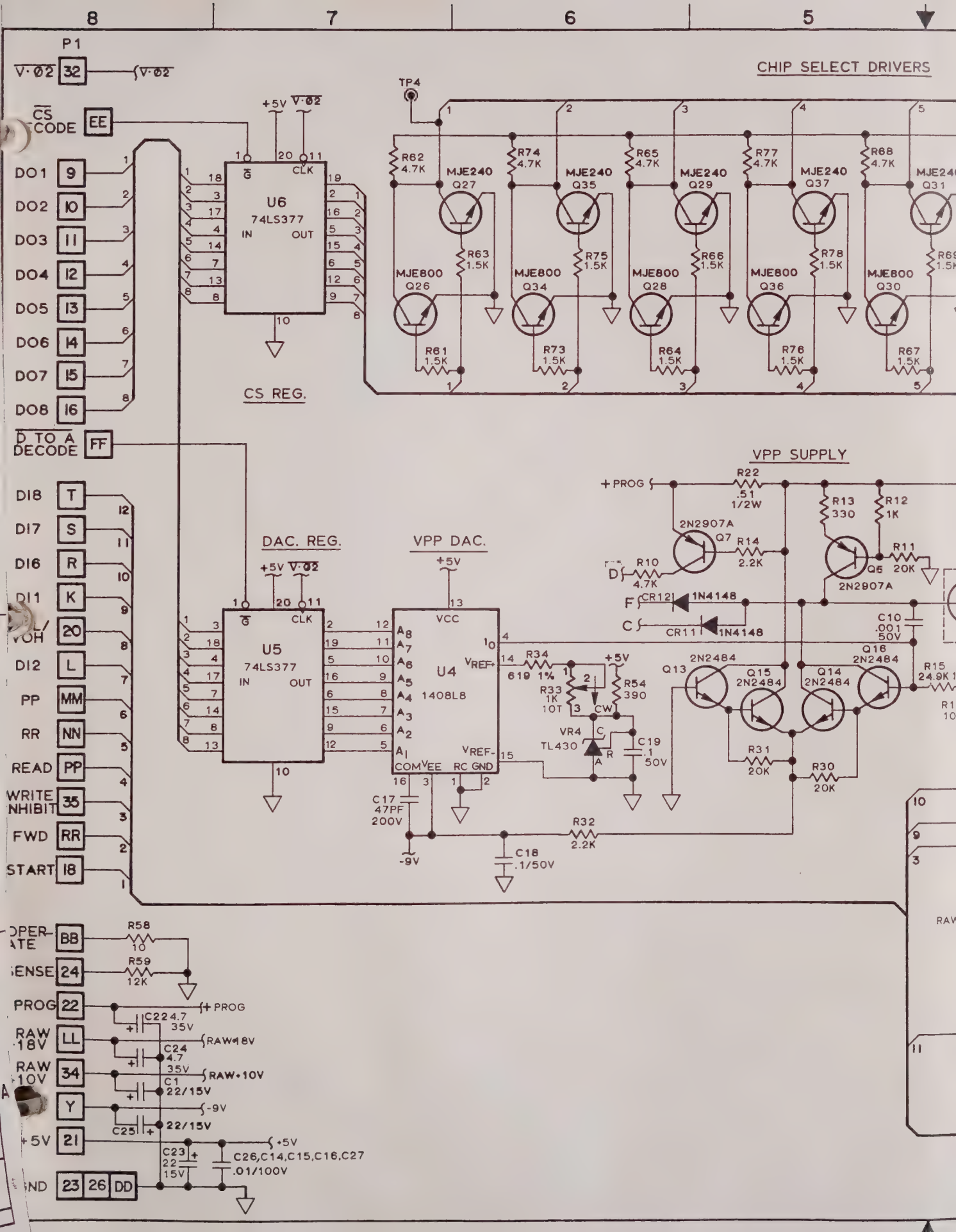
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P1
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CHIP SELECT DRIVERS
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CS CODE
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+5V
U6
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IN
OUT
CLK
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
9
10
11
12
13
14
15
16
CS REG.
D TO A DECODE
FF
R62 4.7K
R74 4.7K
R65 4.7K
R77 4.7K
R68 4.7K
MJE240
Q27
Q35
Q29
Q37
Q31
R63 1.5K
R75 1.5K
R66 1.5K
R78 1.5K
MJE800
Q26
Q34
Q28
Q36
Q30
R61 1.5K
R73 1.5K
R64 1.5K
R76 1.5K
R67 1.5K
VPP SUPPLY
+PROG
R22 .51 1/2W
R13 330
R12 1K
2N2907A
Q7
R14 2.2K
R11
R10 4.7K
Q5 20K
2N2907A
CR12
1N4148
CR11
1N4148
C10 .001 50V
DAC. REG.
U5
74LS377
VPP DAC.
U4
1408L8
VCC
VREF+
VREF-
COM
VEE
RC
GND
R34 619 1%
R33 1K 10T
R54 390
CW
VR4 TL430
C19 .1 50V
C17 47PF 200V
C18 .1/50V
R32 2.2K
-9V
Q13
Q15
Q14
Q16
2N2484
R31 20K
R30 20K
R15 24.9K
DI8
DI7
DI6
DI1
DI2
PP
RR
READ
WRITE INHIBIT
FWD
START
T
S
R
K
L
MM
NN
PP
RR
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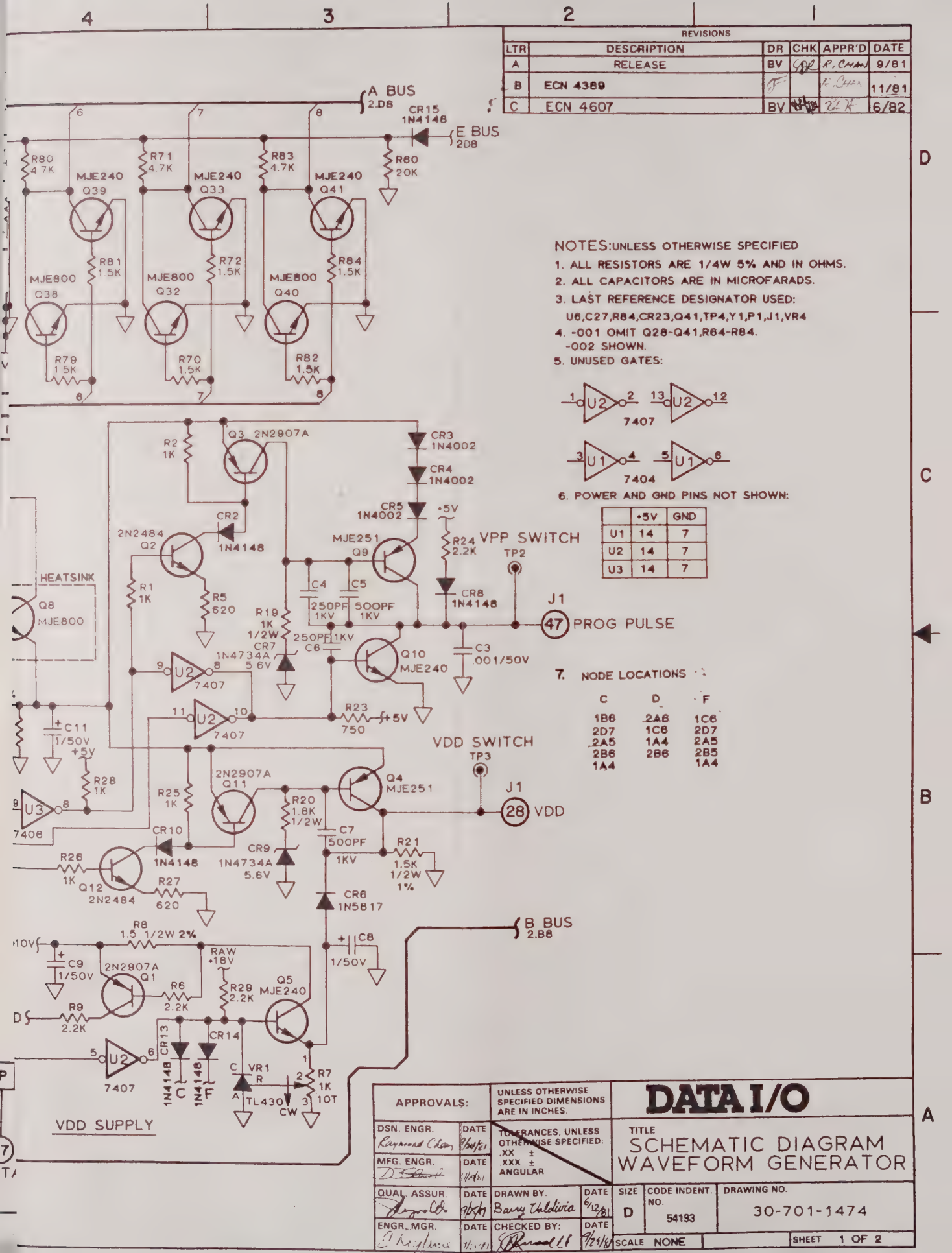
18
20
12
11
10
9
8
7
6
5
4
3
2
1
OPER-ATE
BB
SENSE
24
PROG
22
RAW -18V
LL
RAW +18V
34
RAW +10V
Y
-9V
+5V
21
GND
23
26
DD
R58 10
R59 12K
+PROG
C22 4.7 35V
C24 4.7 35V
C1 22/15V
C25 22/15V
C23 22 15V
C26,C14,C15,C16,C27 .01/100V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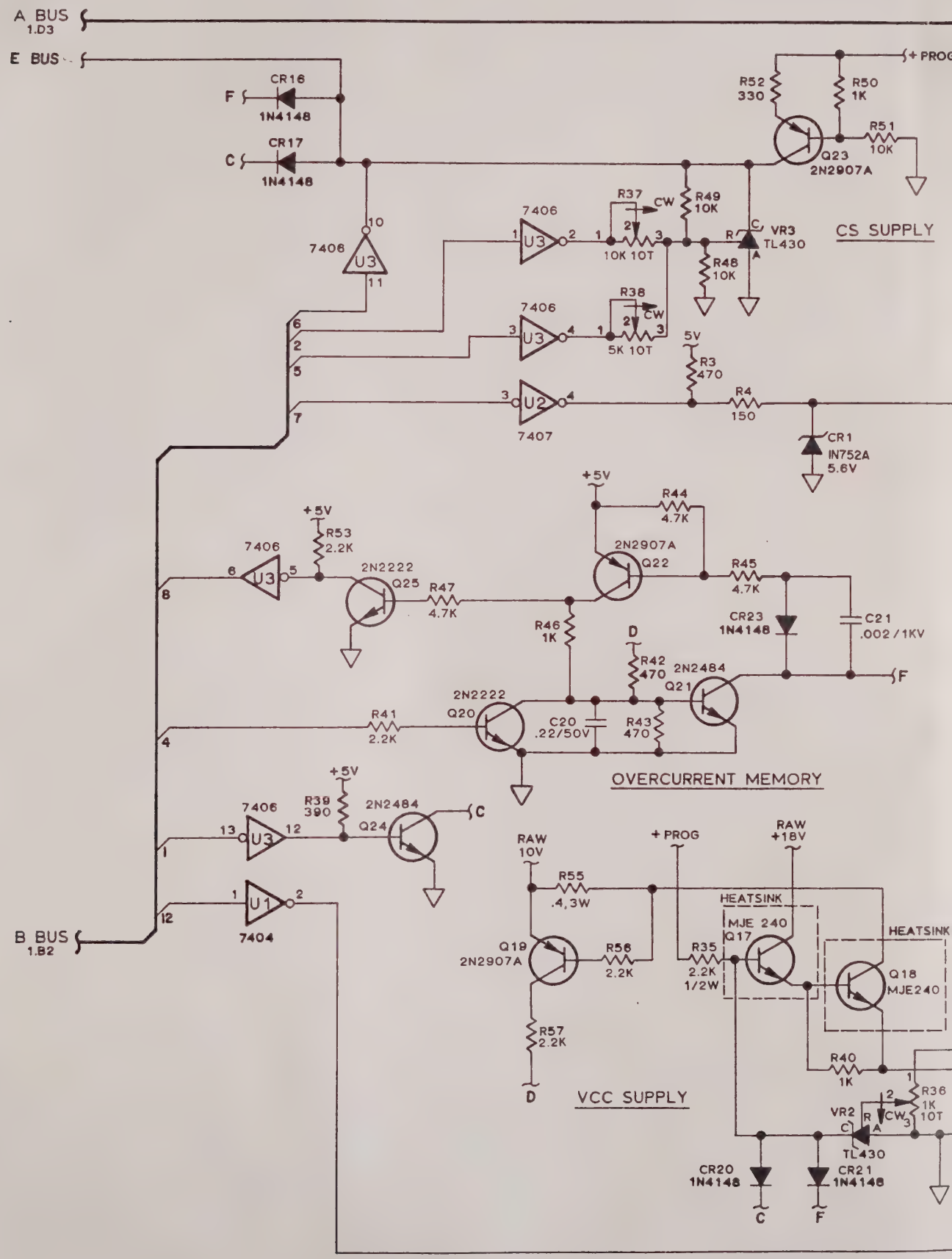
B | ECN 4389 | | | | 11/81
C | ECN 4607 | BV | | | 6/82
A BUS 2.D8
E BUS 2D8
CR15 1N4148
R80 4.7K
R71 4.7K
R83 4.7K
R60 20K
MJE240 Q39
MJE240 Q33
MJE240 Q41
R81 1.5K
R72 1.5K
R84 1.5K
MJE800 Q38
MJE800 Q32
MJE800 Q40
R79 1.5K
R70 1.5K
R82 1.5K
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W 5% AND IN OHMS.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED:
U6,C27,R84,CR23,Q41,TP4,Y1,P1,J1,VR4
4. -001 OMIT Q28-Q41,R64-R84.
-002 SHOWN.
5. UNUSED GATES:
7407
7404
6. POWER AND GND PINS NOT SHOWN:
	+5V	GND
U1	14	7
U2	14	7
U3	14	7
7. NODE LOCATIONS
C: 1B6 2D7 2A5 2B6 1A4
D: 2A6 1C6 1A4 2B6
F: 1C6 2D7 2A5 2B5 1A4
Q3 2N2907A
R2 1K
CR3 1N4002
CR4 1N4002
CR5 1N4002
+5V
CR2 1N4148
2N2484 Q2
MJE251 Q9
R24 2.2K
VPP SWITCH
TP2
HEATSINK
Q8 MJE800
R1 1K
R5 620
C4 250PF 1KV
C5 500PF 1KV
CR8 1N4148
J1
47 PROG PULSE
R19 1K 1/2W
CR7 1N4734A 5.6V
C6 250PF 1KV
Q10 MJE240
C3 .001/50V
U2 7407
C11 1/50V +5V
R23 750 +5V
VDD SWITCH
TP3
R28 1K
2N2907A Q11
Q4 MJE251
R25 1K
R20 1.8K 1/2W
J1
28 VDD
U3 7406
CR10 1N4148
CR9 1N4734A 5.6V
C7 500PF 1KV
R21 1.5K 1/2W 1%
R26 1K
Q12 2N2484
R27 620
CR6 1N5817
B BUS 2.B8
R8 1.5 1/2W 2%
C8 1/50V
C9 1/50V
RAW +18V
2N2907A Q1
R6 2.2K
R29 2.2K
Q5 MJE240
R9 2.2K
CR13 1N4148
CR14 1N4148
VR1 R
R7 1K 10T
TL430 CW
VDD SUPPLY
APPROVALS:
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR
DSN. ENGR. Raymond Chan 9/24/81
MFG. ENGR. 11/4/81
QUAL. ASSUR. 9/8/81
ENGR. MGR. 11/4/81
DRAWN BY. Barry Valdivia 6/12/81
CHECKED BY: 9/29/81
DATA I/O
TITLE
SCHEMATIC DIAGRAM
WAVEFORM GENERATOR
SIZE D
CODE INDENT. NO. 54193
DRAWING NO. 30-701-1474
SCALE NONE
SHEET 1 OF 2

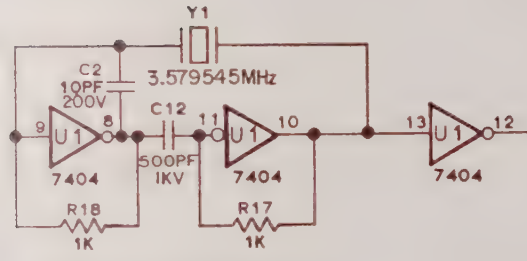

A BUS
1.D3
E BUS
B BUS
1.B2
CR16
1N4148
CR17
1N4148
7406
U3
R37
CW
10K 10T
R49
10K
R48
10K
VR3
TL430
CS SUPPLY
R38
5K 10T
5V
R3
470
R4
150
7407
U2
CR1
IN752A
5.6V
+PROG
R52
330
R50
1K
R51
10K
Q23
2N2907A
+5V
R53
2.2K
2N2222
Q25
R47
4.7K
R44
4.7K
2N2907A
Q22
R45
4.7K
CR23
1N4148
C21
.002/1KV
R46
1K
D
R42
470
2N2484
Q21
F
2N2222
Q20
R41
2.2K
C20
.22/50V
R43
470
OVERCURRENT MEMORY
R39
390
2N2484
Q24
C
U1
7404
RAW
10V
R55
.4,3W
+PROG
RAW
+18V
HEATSINK
MJE 240
Q17
Q19
2N2907A
R56
2.2K
R35
2.2K
1/2W
Q18
MJE240
R57
2.2K
R40
1K
R36
1K
10T
VR2
TL430
CW
CR20
1N4148
CR21
1N4148
VCC SUPPLY

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
	SEE SHEET ONE				

J1

1 — (35) PCS1
2 — (34) PCS2
3 — (33) PCS3
4 — (44) PCS4
5 — (31) PCS5
6 — (30) PCS6
7 — (29) PCS7
8 — (45) PCS8

(46) PGM



CRYSTAL OSCILLATOR

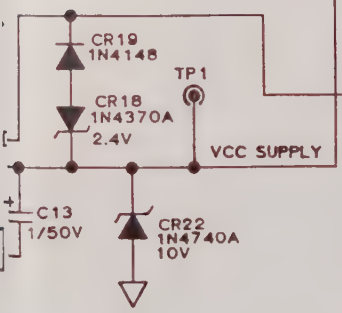
(48) XTAL

(32) VCC

(49) DEVICE PULLUP

(13) (38) (39) GND

(12) VCC SENSE



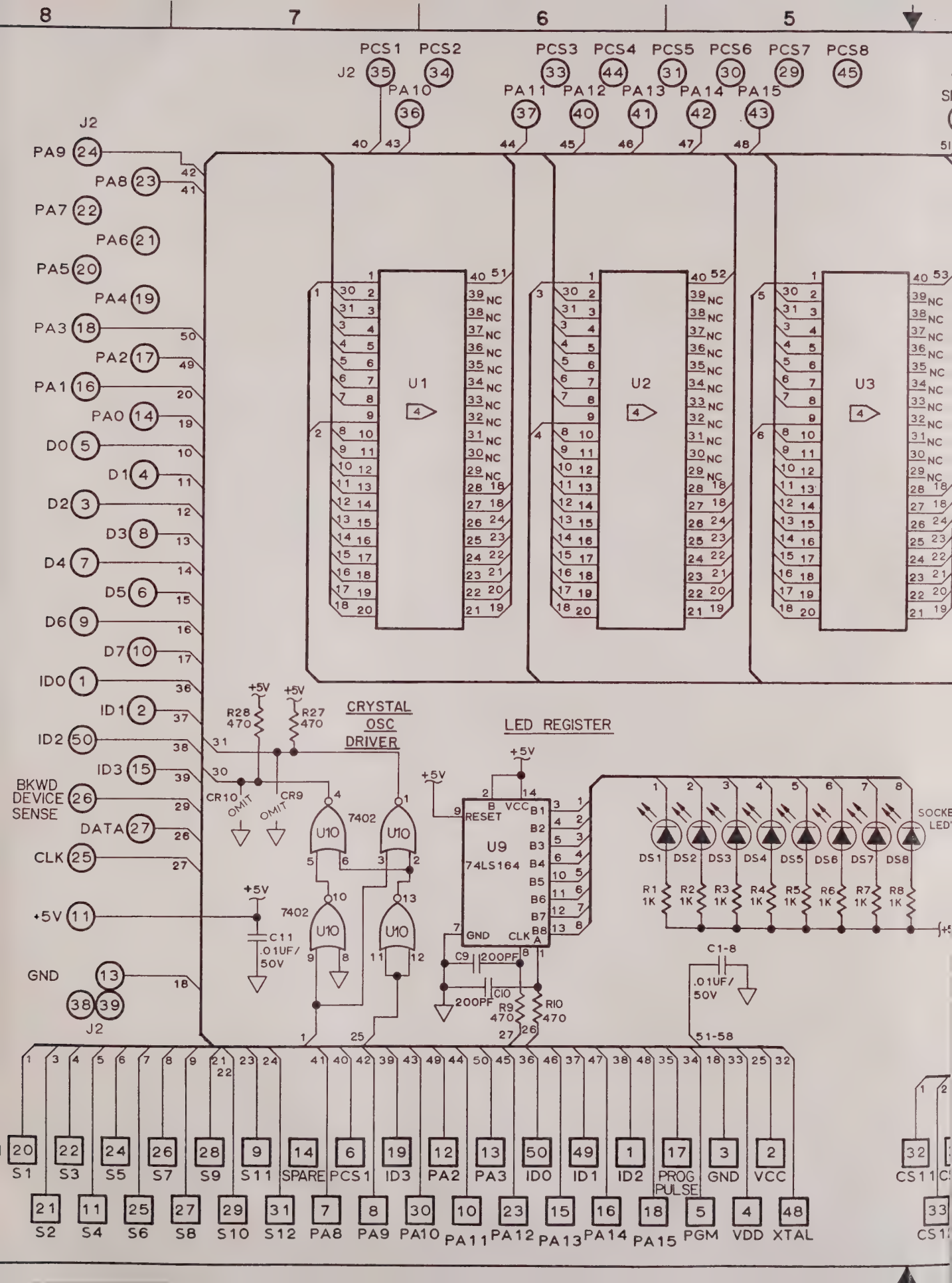
J1 UNUSED PINS

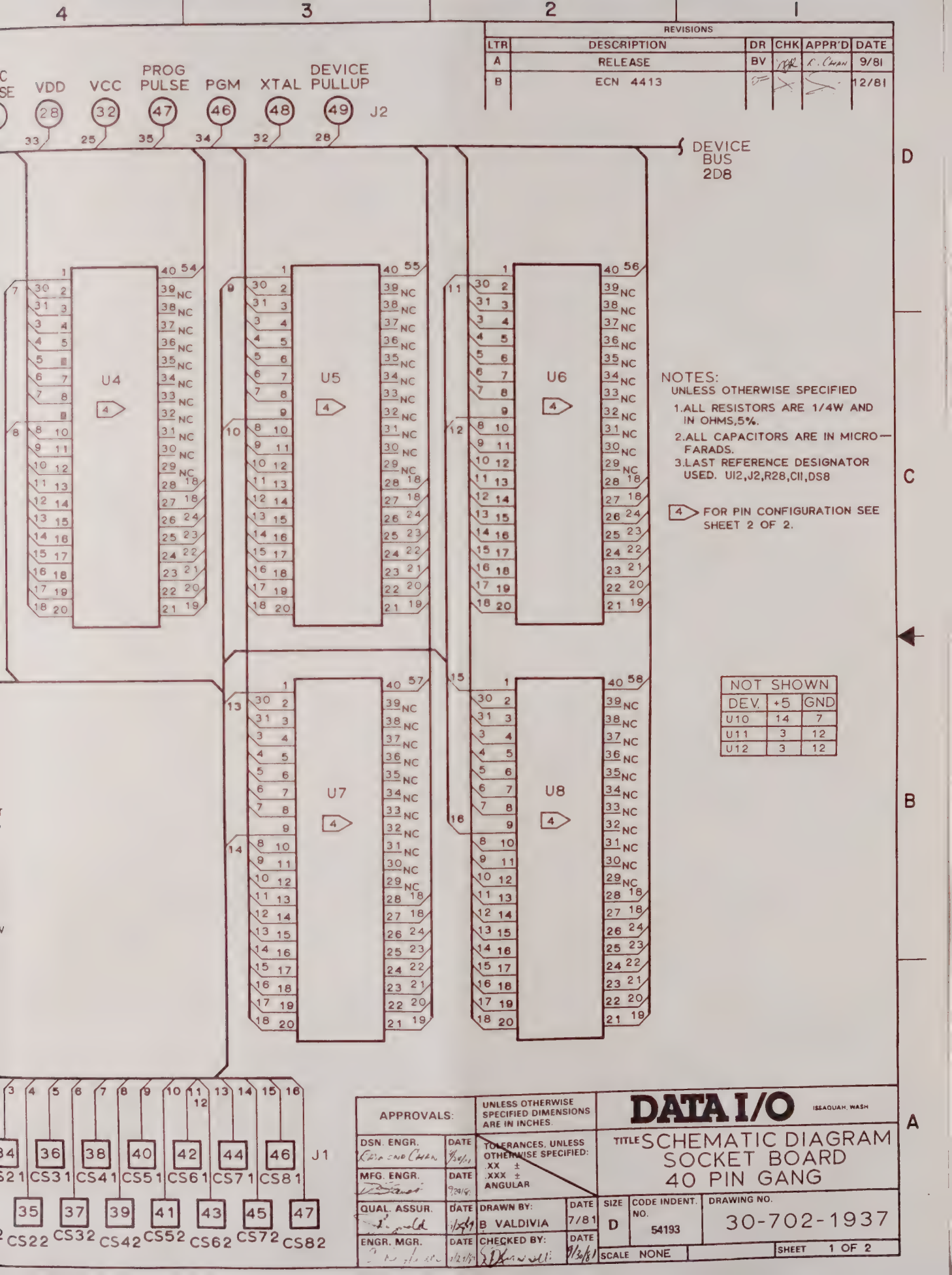
(43) PA 15	(42) PA 14	(41) PA 13	(40) PA 12
(37) PA 11	(36) PA 10	(24) PA 9	(23) PA 8
(22) PA 7	(21) PA 6	(20) PA 5	(19) PA 4
(18) PA 3	(17) PA 2	(16) PA 1	(14) PA 0

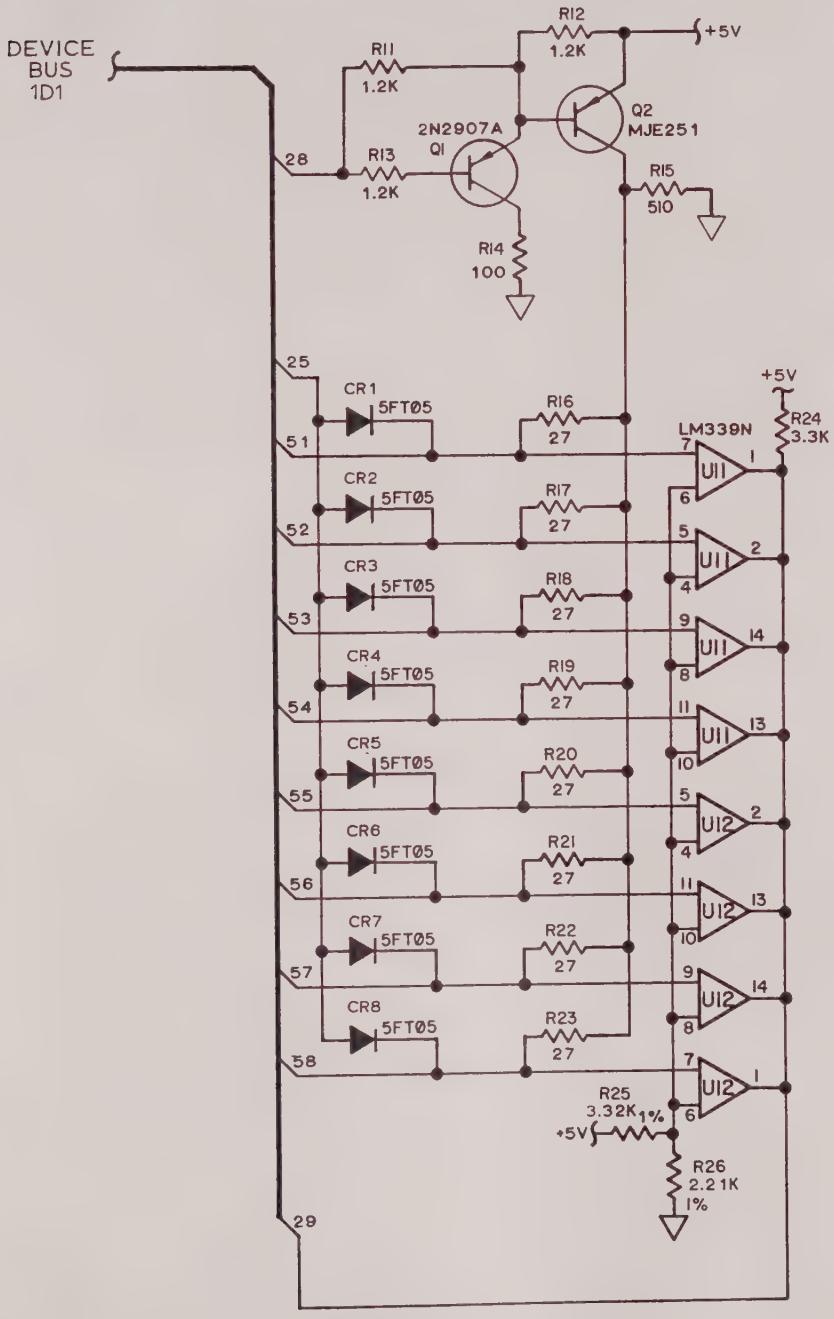
(10) PD 8	(9) PD 7	(8) PD 6	(7) PD 5
(8) PD 4	(3) PD 3	(4) PD 2	(5) PD 1
(27) DATA	(25) CLK	(1) ID 0	(2) ID 1
(50) ID 2	(15) ID 3	(26) BKWD DEVICE SENSE	(11) +5V

D C B A

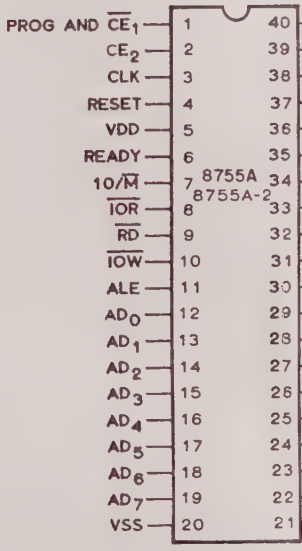
APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O	
DSN. ENGR. Raymond Chan	DATE 9/24/81	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM WAVEFORM GENERATOR	
MFG. ENGR. D. Stark	DATE 11/24/81			
QUAL. ASSUR.	DATE 9/29/81	DRAWN BY: Barry Valdez	DATE 6/12/81	SIZE D / CODE INDENT. NO. 54193 / DRAWING NO. 30-701-1474
ENGR. MGR.	DATE 11/24/81	CHECKED BY:	DATE 9/29/81	SCALE NONE / SHEET 2 OF 2


8
7
6
5
PCS1
PCS2
PCS3
PCS4
PCS5
PCS6
PCS7
PCS8
J2
PA10
PA11
PA12
PA13
PA14
PA15
PA9
PA8
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
D0
D1
D2
D3
D4
D5
D6
D7
ID0
ID1
ID2
ID3
BKWD DEVICE SENSE
DATA
CLK
+5V
GND
U1
U2
U3
NC
R28 470
R27 470
CRYSTAL OSC DRIVER
LED REGISTER
CR10
CR9
OMIT
7402
U10
U9
74LS164
RESET
VCC
GND
CLK
C11 .01UF/ 50V
C9 200PF
C10 200PF
R9 470
R10 470
C1-8 .01UF/ 50V
DS1
DS2
DS3
DS4
DS5
DS6
DS7
DS8
R1 1K
R2 1K
R3 1K
R4 1K
R5 1K
R6 1K
R7 1K
R8 1K
SOCKE
LED'
51-58
S1
S3
S5
S7
S9
S11
SPARE
PCS1
ID3
PA2
PA3
ID0
ID1
ID2
PROG PULSE
GND
VCC
S2
S4
S6
S8
S10
S12
PA8
PA9
PA10
PA11
PA12
PA13
PA14
PA15
PGM
VDD
XTAL
CS11
CS12


4
3
2
1
REVISIONS
LTR | DESCRIPTION | DR | CHK | APPR'D | DATE
A | RELEASE | BV | | K. CHAN | 9/81
B | ECN 4413 | | | | 12/81
VDD
VCC
PROG PULSE
PGM
XTAL
DEVICE PULLUP
J2
DEVICE BUS 2D8
U4
U5
U6
U7
U8
NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICRO-FARADS.
3. LAST REFERENCE DESIGNATOR USED. U12, J2, R28, C11, DS8
4 FOR PIN CONFIGURATION SEE SHEET 2 OF 2.
NOT SHOWN
DEV. | +5 | GND
U10 | 14 | 7
U11 | 3 | 12
U12 | 3 | 12
J1
CS21 CS31 CS41 CS51 CS61 CS71 CS81
CS22 CS32 CS42 CS52 CS62 CS72 CS82
APPROVALS:
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR
DSN. ENGR. DATE
MFG. ENGR. DATE
QUAL. ASSUR. DATE
ENGR. MGR. DATE
DRAWN BY: B VALDIVIA DATE 7/81
CHECKED BY: DATE
DATA I/O ISSAQUAH, WASH
TITLE SCHEMATIC DIAGRAM SOCKET BOARD 40 PIN GANG
SIZE D
CODE INDENT. NO. 54193
DRAWING NO. 30-702-1937
SCALE NONE
SHEET 1 OF 2

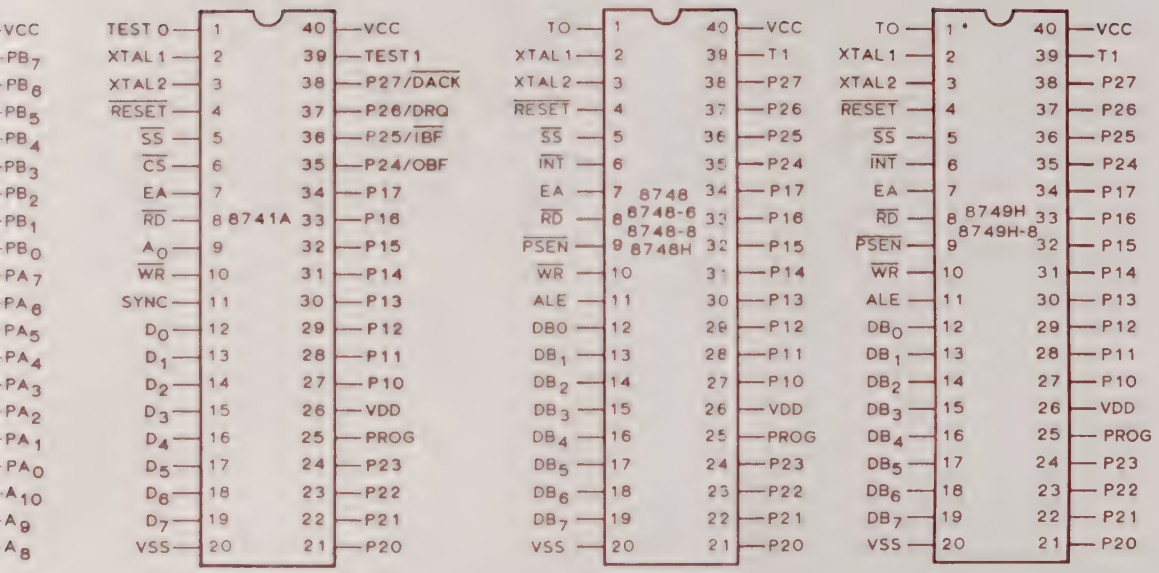


BACKWARD DEVICE DETECT

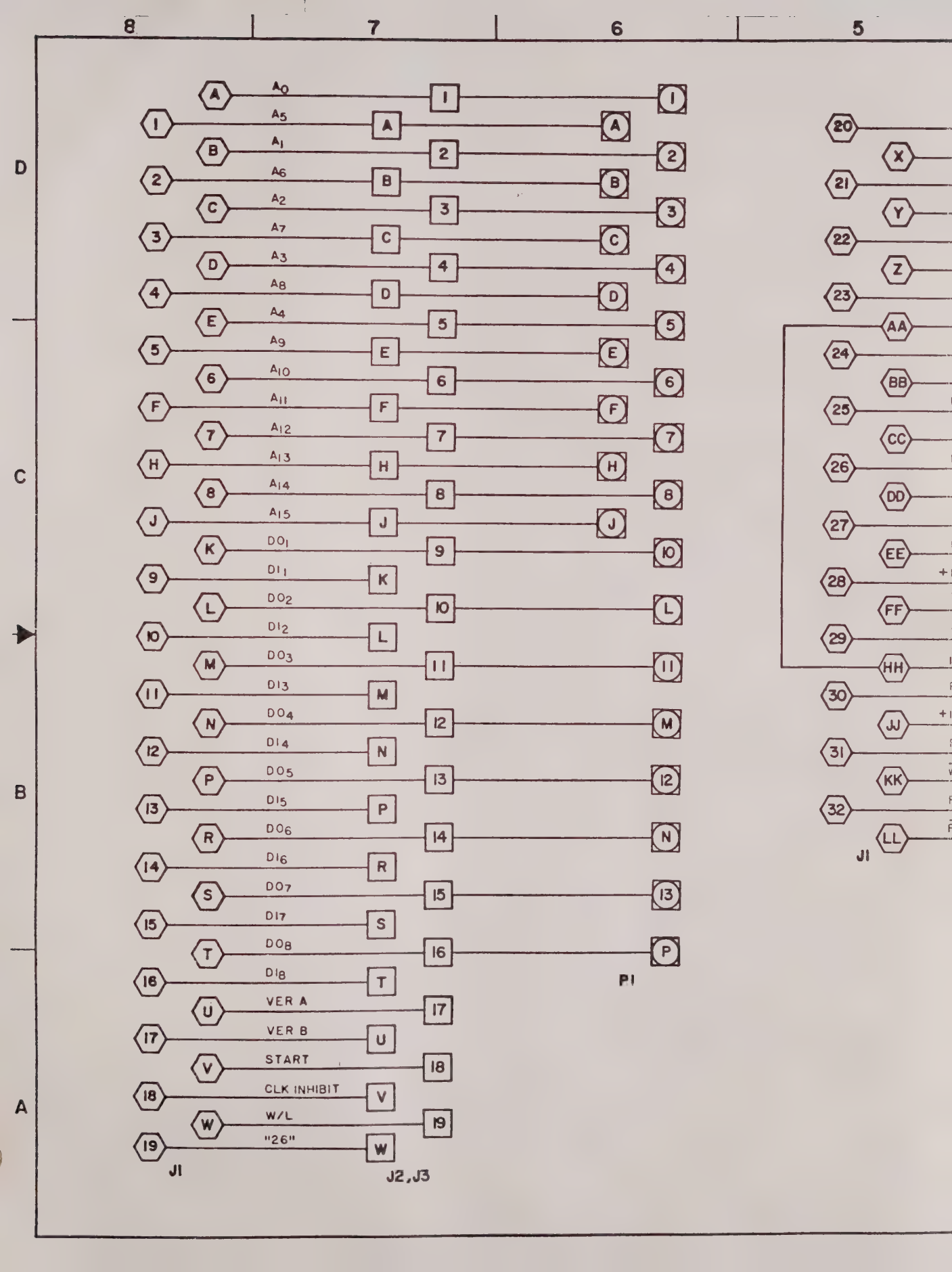


REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
	SEE SHEET ONE				

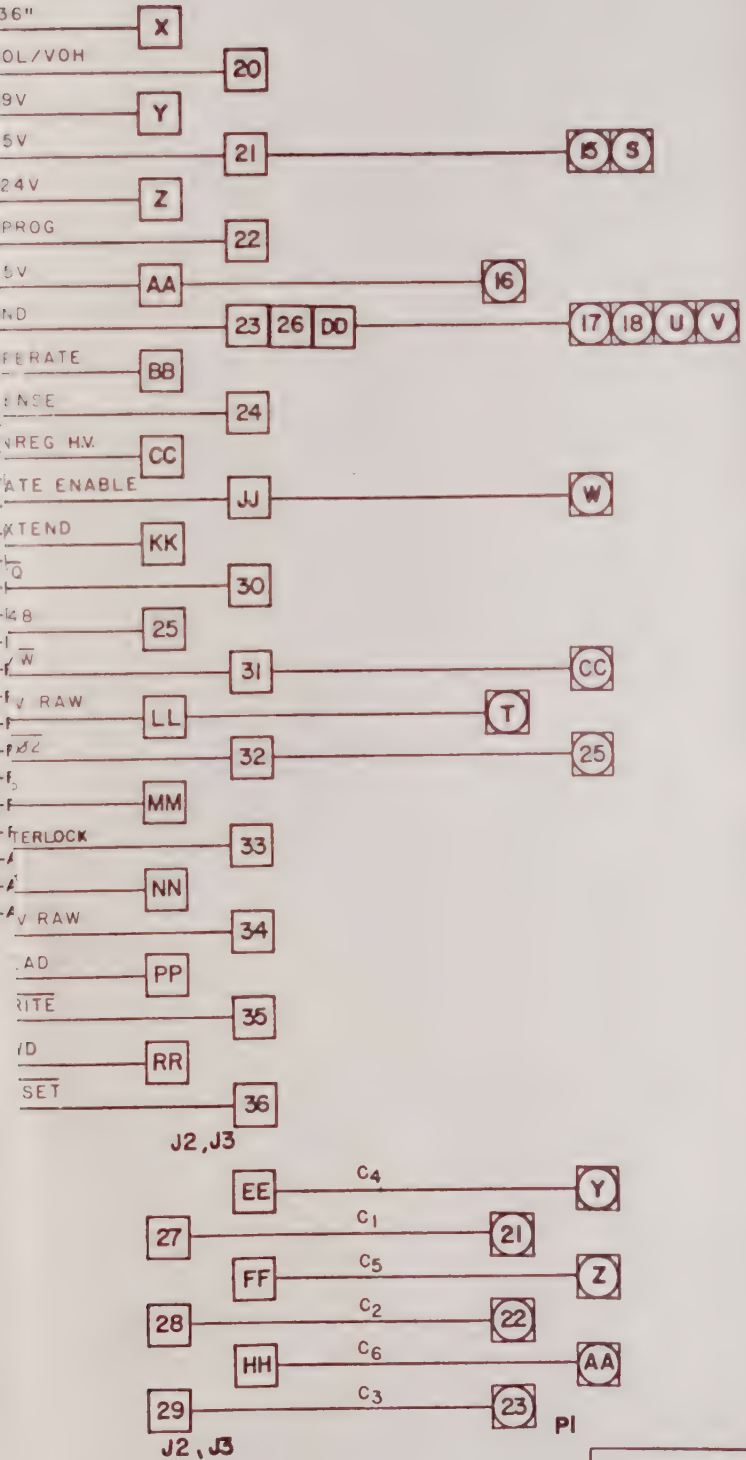
PIN CONFIGURATION



APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.		DATA I/O ISSAQUAH, WASH.			
DSN. ENGR.	DATE	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR		TITLE SCHEMATIC DIAGRAM SOCKET BOARD 40 PIN GANG			
MFG. ENGR.	DATE						
QUAL. ASSUR.	DATE	DRAWN BY: B VALDIVIA	DATE 7/81	SIZE D	CODE IDENT. NO. 54193	DRAWING NO. 30-702-1937	
ENGR. MGR.	DATE	CHECKED BY:	DATE	SCALE NONE		SHEET 2 OF 2	


8
7
6
5
D
C
B
A
A0
A5
A1
A6
A2
A7
A3
A8
A4
A9
A10
A11
A12
A13
A14
A15
DO1
DI1
DO2
DI2
DO3
DI3
DO4
DI4
DO5
DI5
DO6
DI6
DO7
DI7
DO8
DI8
VER A
VER B
START
CLK INHIBIT
W/L
"26"
J1
J2,J3
P1
J1
X
Y
Z
AA
BB
CC
DD
EE
FF
HH
JJ
KK
LL

REVISIONS						
ZONE	LTR	DESCRIPTION	DWN	CK	PE	DATE
	A	RELEASE				1-80
	B	INCORP ADCH A1 PER ECP 0237				5/6/16



P/N 702-1999

APPROVALS	TOLERANCES (EXCEPT AS NOTED)	DATA I/O	
PROJ. ENG.	DECIMAL ±	TITLE	SCHEMATIC DIAGRAM
PROD. ENG.	ANGULAR ±		MOTHERBOARD
CONF. MANG.			
ENG. MGR.	DRAWN BY G. RYDER	SIZE D	CODE IDENT NO / DRAWING NO 008-1999
DATE 1-17-80	CHECK	SCALE NA	SHEET 1 OF 1

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Fax 0118134326094
Telex 2522685 DATAIO J

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090-0014-001

Warranty 90 Days

Data I/O warrants that all equipment sold pursuant to any resultant agreement shall be free from defects in material or workmanship at the time of delivery. Such warranty shall extend for 90 days. Buyer must provide notice to Data I/O within this prescribed warranty period of any defect, if the defect is not the result of improper usage, service, maintenance or installation and equipment has not been otherwise damaged or modified after delivery, Data I/O shall either replace or repair the defective part or parts of equipment or replace the equipment or refund the purchase price at Data I/O's option after return of such equipment by buyer to Data I/O. Shipment to Data I/O's facility shall be borne on account of buyer, including all duties, fees, brokerage and special handling charges. Shipment from Data I/O's facility shall be borne by Data I/O.

(a) Consequential Damages — Data I/O shall not be liable for any incidental or consequential damages incurred as a result of any defect in any equipment sold hereunder and Data I/O's liability is specifically limited to its obligation described herein to repair or replace a defective part or parts covered by this warranty.

(b) Exclusive Warranty — The warranty set forth herein is the only warranty, oral or written made by Data I/O and is in lieu of and replaces all other warranties, expressed or implied, including the WARRANTY OF MERCHANTABILITY AND THE WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE.

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Reader Comments
Applications Manager
10525 Willows Road N.E.
C-46
Redmond, WA 98052

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UNITED STATES

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Warranty/Registration
Service Manager
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C-46
Redmond, WA 98052

Reader Comments

The manual's completeness, accuracy, organization, usability, and reliability: _____

_____

Did you find errors in this manual? _____

How can this manual be improved? _____

_____

_____

Additional comments: _____

_____

Name _____ Title _____

Department _____ M/S _____

Company _____

Address _____

City _____ State _____ Zip _____

Phone ( ) _____

Manual or Part No. _____

Warranty/Registration

Please return this card to Data I/O within five days

Did the packaging of this equipment exhibit any outward signs of physical damage? ☐ YES ☐ NO

Did this equipment arrive intact, without loose parts or cable damage? ..... ☐ YES ☐ NO

Did the equipment operate on power-up? ..... ☐ YES ☐ NO

Did you attain adequate system performance? ..... ☐ YES ☐ NO

Were any electrical adjustments required? ..... ☐ YES ☐ NO

If you required assistance, was a local Data I/O representative contacted? ..... ☐ YES ☐ NO

Comments: _____

_____

Name _____ Title _____

Department _____ M/S _____

Company _____

Address _____

City _____ State _____ Zip _____

Phone ( ) _____

Model or Description _____ Serial or Part No. _____

Date Received _____

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